PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3: A61B 5/04

A1

(11) International Publication Number: WO 81/02832

(43) International Publication Date: 15 October 1981 (15.10.81)

(21) Int. Application Number: PCT/US81/00419

(22) Int. Filing Date: 31 March 1981 (31.03.81)

(31) Priority Application Numbers: 136,044
145,335

(32) Priority Dates: 31 March 1980 (31.03.80)
30 April 1980 (30.04.80)

(33) Priority Country: US

(71) Applicant: DATAMEDIX, INC. [US/US]; Arvida Park of Commerce, 1001 N. W. 58th Street, Boca Raton, FL 33431 (US).

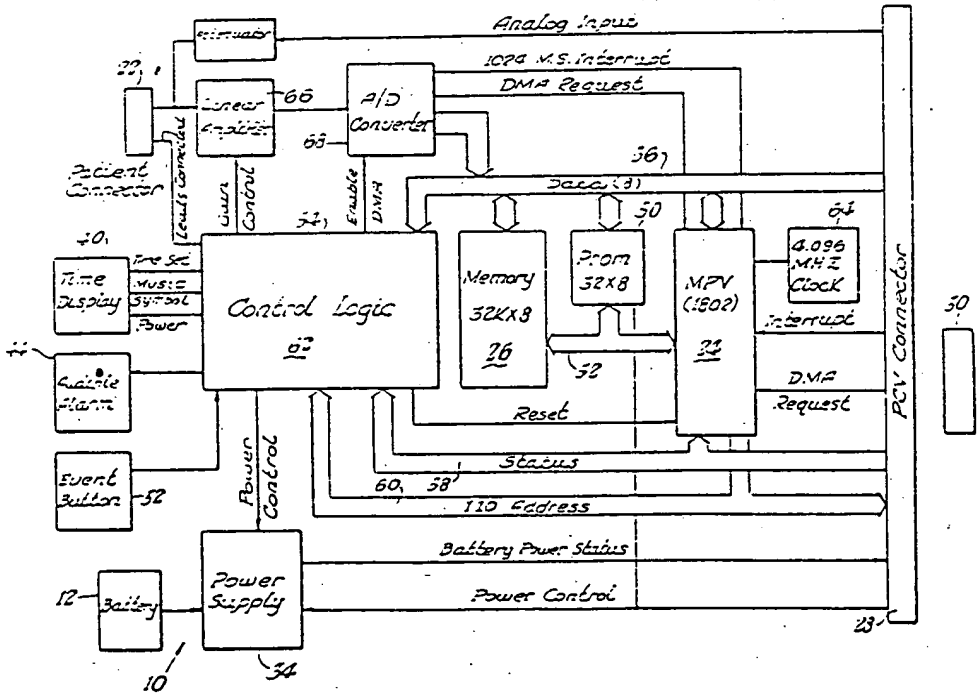
(72) Inventors: MOUNT, Joseph, Franklin; 2250 Cherry Palm Drive, Boca Raton, FL 33432 (US). JOHNSON, Robert, Joel; 2955 N. E. 19th Street, Pompano Beach, FL 33305 (US). SCHELL, James, Joseph; 400 S. E. 5th Terrace, Pompano Beach, FL 33301 (US). POUMAKIS, Eleuthere; 6625 Paul Mar Drive, Lantana, FL 33462 (US). PLUMMER, David, John; 2511 N. E. 33rd Street, Lighthouse Point, FL 33064 (US). SCHUETTPELZ, Keith, Neil; 1977 Bethel Boulevard, Boca Raton, FL 33432 (US). MITTNACHT, David, Alan; 4577 Sugar Pine Drive, Boca Raton, FL 33431 (US). TRAXLER, John, Douglas; 380 N. E. 36th Street, Boca Raton, FL 33431 (US). SINCLAIR, John, Walter; 3120 N. W. 67th Court, Fort Lauderdale, FL 33309 (US). SHAH, Atul; 4520 N. W. 36th Street, Lauderdale Lakes, FL 33319 (US). BRUCE, Robert, Ewing; 1010 S. W. 2nd Street, Boca Raton, FL 33432 (US). EDWARDS, Craig, Martin; 9355 S. W. 8th Street, Boca Raton, FL 33432 (US). DAVIS, Jonathan, Butler; 1151 N. W. 6th Avenue, Boca Raton, FL 33432 (US). MUIR, Malcolm, Douglas; 10340 N. W. 44th Street, Coral Springs, FL 33065 (US).

(74) Agent: MALIN, Eugene, F.; Malin & Haley, One Financial Plaza, Suite 2400, Fort Lauderdale, FL 33394 (US).

(81) Designated States: AT (European patent), AU, BR, CH (European patent), DE (European patent), FR (European patent), GB (European patent), HU, JP, KP, NL (European patent), SE (European patent), SU.

Published
With international search report

(54) Title: MEDICAL MONITOR



(57) Abstract

A heartbeat analyzer includes and ambulatory unit (10) carried by the subject and having a microprocessor (24) controlling flow of data from the pickup leads (16, 18, 20) to the storage means (26) for up to 72 hours accumulation of data and analyzes the data with respect to rate rhythm and shape. An interface circuit (28) is provided to read out the stored data at a later time. A second unit (30), to which the first unit is connected (84) for data transfer, provides for display of the stored data (display) and for entering (keyboard) data corresponding to normal conditions of a heartbeat for use as a standard of comparison by the ambulatory unit (10).

Medical Monitor

Technical Field

This is an electrical analyzing system for an ambulatory patient including a fixed base procedure control system and a dockable programmable ambulatory satellite unit. In particular it is an electrocardiogram analysis system that includes the programmable ambulatory monitoring unit (AMU) that provides an in depth report and the programmable procedure control system that provides an in depth report display. The procedure control system (PCS) includes a base procedure control unit (PCU) and a procedure report printer.

The dockable ambulatory monitoring unit is an ambulatory, electrocardiogram monitoring, real-time analysis and storage device for use by cardiologists, internists, and physicians to perform long term monitoring and analysis of ambulatory patient's electrical signals. The ambulatory monitoring unit includes electrical leads, A/D converter, a programmable microprocessor, control circuits with noise management, signal identification and pattern classification, digital memory, prom, power management circuit, digital storage means, audio indicator, visual time indicator, a patient event switch, electrodes connection circuit for docking the unit to the procedure control unit, and a power source. The ambulatory monitoring unit analyzes each individual heart beat, defines a normal beat and abnormal variations, tabulates and sorts the occurrences, and if there are significant changes in rate, rhythm or shape, retains a copy of the actual waveform series in storage.

Background Art

This invention relates to an analysis system including a programmable ambulatory monitoring unit for receiving, providing real-time analysis and storing information relating to electrical signals generated by a patient's body and for immediate display when docked with a procedure control system for professional use.

Various types of monitors have been suggested in the past, most of them in the form of ECG computers for in-hospital use. Some portable monitors have been designed with magnetic tapes for storage of analogue data or radio transmission means for transmitting analogue data to a remote unit.

By way of example, U.S. Patent No. 3,267,934 discloses an electrocardiographic means for receiving an electrocardiac signal and magnetically recording the signal on a magnetic tape for reproduction in the same state at a future time. U.S. Patent No. 3,832,994 discloses a similar means of providing an analog electrocardiac signal in a first unit, but with an FM transmitter disposed in the first unit for transmission of the analog signal to a second non-ambulatory unit which is remote from the first unit and where the analog signal is converted in the non-ambulatory unit to a series of digital pulses for processing.

All of the ambulatory or portable prior art devices have no way to process the analog signals received from the patient during real-time, that is, in use time. The present invention processes, analysis and stores the data in the ambulatory

unit for immediate retrieval and display of the data when the ambulatory unit is docked so that a physician has immediate access for professional interpretation in patient management. In addition, the prior art ambulatory or portable devices do not appear to be capable of detection, noise management, real-time analysis, classification of input, and capable of being programmed to vary the data items to be classified and stored to individualize the ambulatory monitoring unit prior to the patients' use. System architecture is such that future modifications over a wide range of applications can be accomplished with software changes. Since the electrocardiogram analysis system is fully programmable, changes in analytical software approaches among Cardiologists can be implemented in a reasonably straightforward manner.

Disclosure of Invention

, A fixed base - dockable satellite analysis system for providing immediate in-depth report of the results of the real-time monitoring of ambulatory patient's electrical output signals for example electrocardiogram signals. The analysis system includes a programmable ambulatory monitoring unit (AMU) and the programmable procedure control system that provides an in depth report display when the AMU is docked.

The ambulatory monitoring unit (AMU) is designed to monitor, detect, analyze in real-time, and report on an ambulatory patient's electro-cardiogram (ECG) signals taken from a modified lead

electrode configuration. The unit provides real-time processing of modified ECG signals, patient convenience features, and comprehenisve ECG analysis. The monitoring is performed by a small, light weight, ambulatory monitoring unit. The monitoring includes acquisition and conditioning through patient electrodes, electric leads, ECG amplifier filters and analogue-to-digital (A/D) converter and control means. The control means includes control logic, memory and microcomputer. An ECG data buffer is connected between the A/D converter and the control means. The ambulatory monitoring unit is designed to detect significant changes in rate, rhythm and/or shape of the patient QRS complexes. The QRS complex, an electrocardiogram wave pattern, is caused by ventricular depolarization. The QRS identification is accomplished in the same time frame through the control means by QRS detection management, QRS detection and feature extraction, noise management, and QRS peak detection and counting. The QRS detection and feature extraction the output is then passed through the QRS template management. The noise management designates low noise to QRS detection and feature extraction, designates moderate noise to QRS detection and correlation with QRS types, designates high noise for skip and skip recording. The QRS template management and QRS detection and correlation with QRS types data is processed to classify the QRS patterns, such as single beat patterns, multibeat patterns, shape changes and rate and rhythm changes. The classified QRS patterns

are stored for immediate display of a record after docking.

In addition, the analysis display or reports may include the presence of S-T elevations and depressions, missed beats, asystole and patient activated symptomatic events. The patient may record an event alert through the manual controlled event button.

Therefore, the ambulatory monitoring unit (AMU) is a portable, microcomputer-based device that detects the patient's ECG, classifies the QRS complexes individually and in sequence, then stores the results for subsequent generation of a summary report by the PCS. The ECG analysis is designed to detect significant changes in rate, regularity and/or shape of the QRS complexes. In general, the system devises a template of the patient's typical QRS complex. This complex is then used as a reference for recognition of QRS complexes. QRS complexes which do not match the reference complex are subjected to comprehensive shape analysis. Individual QRS shape, time position with respect to adjacent complexes and patterns of QRS shape and time position are used to identify atypical ECG phenomena. Atypical results are stored in memory on a priority-retention basis. Up to 30 types of single-beat changes and as many as 26 combinations of atypical cardiac occurrences are identified for reporting.

During the ambulatory monitoring procedure, the operation of the ambulatory monitoring unit (AMU) is directed by a control means that may be a hard wired control or a computer program which resides in the ambulatory monitoring units memory.

This control means is also referred to as the electrocardiogram monitoring and analysis means, receives input from the ambulatory patient's electrocardiogram signals, input from the ambulatory monitoring unit electronic components and input from the patient event switch. These inputs are used to control the processing of ECG monitoring and analysis means. The results of the electrocardiogram analysis performed by ECG monitoring and analysis means in real time, that is, ambulatory time, are recorded in the ambulatory monitoring unit storage. It is this digital data that is used to construct the final report in the PCS.

ECG monitoring and analysis means, by analyzing the various inputs from the ambulatory monitoring unit components, is designed to determine that the monitoring procedure must be terminated because of insufficient power. In this case the ECG monitoring and analysis means can place the ambulatory monitoring unit into a Data Save mode which preserves the analysis data which has already been generated and stored.

The ambulatory monitoring unit thus provides a vehicle for the ECG monitoring and analysis means while it performs the ECG analysis. The ambulatory monitoring unit provides the facilities for collecting and conditioning the ECG signal that is to be analyzed by the ECG monitoring and analysis means. The ambulatory monitoring unit provides the interface to direct patient in regard to input and time readout through professional controls. The ambulatory monitoring unit provides an interface to the procedure control unit (PCU).

The ambulatory monitoring unit is a battery operated, 24 hour and longer ambulatory heart monitor. All the electronic circuitry, memory, and power supply items are contained within this single envelope supported by a carrying case. The ambulatory monitoring unit monitors the patient's electrocardiogram activity via a single channel (two leads) connection employing a three patient lead that also includes a reference connection. The microprocessing unit including a random access memory continuously analyses the patient's heart activity during the enter monitoring period of the ambulatory patient. When the abnormal activity is detected, the microprocessing unit stores data in memory relating to the detected abnormalities. The ambulatory monitoring unit is docked at the end of the monitoring period in a procedure control unit (PCU) through the procedural control unit connectors. When the ambulatory monitoring unit is connected to the procedural control unit a visual and/or printed report may be immediately generated since the analysis has already taken place in real-time.

The controlling component is a microprocessing unit which directly accesses all of the memory and prom through a plurality of connections. The prom is acceptable only when the ambulatory monitoring unit is docked into the process control unit and automatically powered by the process control unit with a fail safe system. The microprocessing unit via programmed I/L using a data bus, a status bus, and I/L address bus. The microprocessing unit disclosed herein may operate on a 4.096 MHZ clock

which results in a memory cycle time of 1.953 microseconds.

In the preferred AMU, the ECG amplifier includes two stages of amplification followed by a notch filter and a gain-programmable amplifier. This amplifier chain exhibits high common mode rejection and limits the input amplifier leakage current to the patient to less than 10 nanoamperes. The notch filter suppresses pickup of the power line frequency.

The amplified ECG signal is sampled at regular intervals, converted to its digital equivalent and then placed in memory all under the control of the AMU microprocessor. The operation of the microprocessor is directed by a computer program which resides in the AMU memory. The operation of this device may be operated for any number of channels by duplicating the input amplifiers, the A and D converters, and the ECG data buffers and utilizing duplicate software such as illustrated and shown in Figure 8B. A single channel is illustrated in Figure 8B. This program examines the digitized ECG signals for rate, regularity and/or shape conformance. For example a 20 second data examination cycle may be used. Atypical QRS complexes are retained in memory on a priority classification basis; that is, complexes containing minor aberrations are automatically discarded in favor of those having more severe irregularities. It is this data, appropriately structured and formatted, which comprises the report that is generated for the physician at the end of the procedure.

The computer's input and output control logic provides interfaces to the various auxiliary devices within the AMU such as the A/D converter, microprocessor, etc. This circuitry is used during AMU initialization to make a software-controlled adjustment of the ECG amplifier gain.

It is also used during synchronization of the LCD time display, activation of the audible signal, mode control of the DC power source and for general housekeeping routines. Additionally, the control logic provides a patient interface to allow the entering into memory of Symptom switch depressions as identification of specific, patient-observed, physiologic discomfort periods.

The DC power source consists of two 9-volt alkaline batteries connected in parallel. This power source is capable of sustaining AMU operation during ECG monitoring and analysis for a minimum of 26 hours. Following the procedure period, the AMU power source is able to preserve the results in memory for an additional period of 72 hours after battery "end-of-life" has been detected by the control logic; this is the data-save period.

Two, distinctively different audible signals are emitted to alert the user of an abnormal operating condition. For a low power warning, a continuous tone is sounded for five seconds. A disconnected patient lead or an excessive input noise condition is identified by an interrupted tone for a period of about 20 seconds. In the case of noise, the signal recurs at one minute intervals until the noise subsides. For a disconnected lead, the signal is not repeated.

Prior to use, the AMU is initialized by inserting it into the "docking" receptacle of the Procedure Control Unit. When the unit is docked, the timing/control interface signals permit the orderly transfer of PCU program data into the AMU memory for subsequent use during ambulatory operation. Also, at this time, the AMU power source is checked

under load and the LCD time display is synchronized to the current time-of-day via a master timing reference contained in the PCU. As part of the "docking" process, operation of the AMU is automatically switched over from battery power to PCU power in order to conserve battery power.

Two chest electrodes or leads per channel are required and an additional lead is required for a reference. In the system illustrated in Figure 1, three chest electrodes are connected to the PCU via a patient cable are used to sense the patient's ECG. The ECG signal is routed through an isolation amplifier in the PCU before being applied to the AMU.

At this point, the signal passes through the AMU ECG amplifier where the proper programmable gain factor is introduced. Next, the ECG signals are digitized, entered into memory and analyzed to determine the patient's typical, that is the patient's most common occurring QRS complex. After selection, the typical QRS complex is routed back to the PCU for inspection and approval by the physician. If accepted, the initialization process is completed; otherwise, the AMU will discard the first selection and present its second choice as a typical QRS complex. This process is repeated until the physician is satisfied with the AMU's selection.

Remote initialization from the PCU can also be accomplished by connecting the electrode set to the patient and allowing the AMU to select a typical QRS. In the event that the selected QRS is not the patient's typical QRS, the AMU will establish the most popular QRS as the typical QRS. The AMU becomes a self initializa device.

Also as part of the initialization process, the name of the patient, time-of-day, date and the various

system options selected are transferred into the AMU memory. In the self initialization mode or device this data or statistical data will be put in prior to the distribution of the AMU and prior to connection to the patient. Once the initialization process is completed, the AMU is undocked from the PCU, the patient cable connections are transferred from the PCU to the AMU and ambulatory monitoring may begin.

The PCS is a desk-top, miniaturized computer system consisting of a keyboard/display device and a separate graphics-quality printer. Both devices are powered directly from a standard AC power source and employ individual switches to control the application of power.

The keyboard/display device contains the microcomputer and provides a receptacle or port for "docking" the Ambulatory Monitoring Unit. In addition, this device displays service lists which prompt the operator in the use of the system. The keyboard provides a means by which the operator communicates with the computer. The graphics-quality printer supplies a hard copy report of the results of the ambulatory procedure. For patient safety, during AMU initialization, the patient's ECG signal is passed through an isolation amplifier contained in the AMU analog interface section. The buffered ECG signal is routed from the patient through the PCU docking receptacle and to the AMU where it is digitized.

The procedure control system PCS includes an AMU digital interface with a line drivers and receivers which buffer the signals to and from the docked AMU during the reporting phase of the AMU and the loading of software instructions.

Additionally, this interface permits monitoring of the AMU battery status and the application of PCU power to operate the AMU during docking. Also included in the PCU is a solenoid which releases the AMU from the "docked" position. Upon user request, this solenoid can be energized forcing the AMU away from the docking receptacle and allowing the unit to be manually withdrawn by the user.

The buffered, digital AMU signals are interfaced with the PCU system bus by the I/O logic. This section controls the transfer of the contents of the AMU, the ECG analysis program, and the system diagnostics to and from the PCU.

The program memory consists of EPROMs which contain the resident program used during ECG analysis as well as display related programs which "prompt" the operator in the use of the system.

When power is first supplied to the PCU, basic test routines are activated to briefly check the main components of the system. System diagnostics contained in an auxiliary EPROM module permit a thorough test of the system as well as providing fault location for module replacement. An LED display, together with CRT diagnostic error messages, assist in localizing the problem to a specific area.

The keyboard section includes alphanumeric and function keys which permit the user to select specific services, enter patient/physician data,

make procedure annotations, edit test results, modify test routines, etc. The keyboard entries are decoded and the associated request/commands are routed to the appropriate device via the system bus.

The patient's summary report is printed out on an electrosensitive, graphics-quality printer. A complete page is printed in approximately 10 seconds. Two horizontal dot resolutions are employed during the printing cycle. The lower resolution is used for the alphanumerics and the higher density is necessary for graphics reproduction.

The printing cycle can be started and stopped at the end of the page via a keyboard entry; however, paper feed, character/graphics printing and paper cutting are all controlled automatically by the program.

The data displayed on the CRT monitor is derived from three separate memories: graphics, grid and alphanumerics. The contents of these memories are read out and summed in a video driver stage before being applied to the raster-scan monitor. The monitor presents the user service-selection menus and provides a high resolution display of static and dynamic ECG data. For a static display, either a grid or calipers can be superimposed on the ECG waveform to assist in the analysis of the data; also, the displayed data can be expanded for closer observation.

It should be noted that the output information from the preferred AMU from the PCS is as follows:

1. A calibration strip (the calibration strip is a graphical presentation of ECG information as well known and commonly used) shows amplifier gain settings and selected typical QRS complex.

2. Every anomoly deviating from the typical selected QRS complex is stored in memory as a template which is generally of a one second duration.

3. Statistical data of patient.

4. ECG graphical strip.

5. Up to forty ECG strips representing observed rate, rhythm and shape anomolies.

6. Histrogram (a bar chart versus time) showing time of events of graphically depicted items referred to in paragraphs 4 and 5 above.

7. Histrograms; rate information versus time showing maximum averages and minimum rate over program intervals.

8. Histrograms of ST segment deflection versus time over programmable intervals.

9. Histrograms of major events such as:

a. Premature ventricular occurences (PVC's)

b. Bigeminy, trigeminy occurrences etc.

c. Couplets occurrences etc.

d. All major events of rate, rhythm and shape are producible in histrogram form.

10. Tabular data of all histrogram data also printed out at physician's discretion in tabular form.

It is an object of the invention to derive data from an ambulatory patient's ECG signal and analyze each ECG waveform in real time and retain the results in a small, lightweight ambulatory satellite computer and then at the conclusion of the monitoring period, the stored results are printed out in comprehensive report form by a companion or base desk-top unit.

Other objects and advantages of this invention will be apparent from the following description, the accompanying drawings and the appended claims.

Brief Description of Drawings

In the drawings:

Figure 1 is a block diagram of the ambulatory monitoring unit and illustrating the procedural control unit.

Figure 2 is an illustration of a patient and electrocardiogram connections.

Figure 3 is a time sequence graph.

Figure 4 is a schematic of the logic data board.

Figures 5A through 5B are schematic drawings of a portion of the logic microprocessing unit.

Figures 6A through 6B are schematic drawings of an additional portion of the logic microprocessing unit.

Figures 7A through 7B are schematic drawings of logic, 16 K memory.

Figure 8A is a general view of the present invention.

Figure 8B is a flow diagram of the data and controls of the present invention.

Figure 9 is a block diagram of the Procedure Control System of the present invention.

Figure 10 is a block diagram of the present invention.

Figure 10A is a block diagram of the System Interconnect of the present invention.

Figure 11 is an overview of the CPU of the Procedure Control System of the present invention.

Figure 11A is a block diagram of the CPU of the Procedure Control System of the present invention.

Figure 12 is a display memory overview of the Procedure Control System of the present invention.

Figure 12A is a block diagram of the display memory of the Procedure Control System of the present invention.

Figure 13 is an overview of the CRT control of the Procedure Control System of the present invention.

Figure 13A is a block diagram of the CRT control of the Procedure Control System of the present invention.

Figure 14 is an EPROM block diagram of the Procedure Control System of the present invention.

Figure 15 is an input/output overview of the Procedure Control System of the present invention.

Figure 15A is a block diagram of the input/output brand of the Procedure Control System of the present invention.

Figure 16 is a block diagram of the non-volatile memory of the Procedure Control System of the present invention.

Figure 17 is a block diagram of the ambulatory Monitoring Unit interface of the Procedure Control system of the present invention.

Figures 18A-18K are the timing charts of the Procedure Control System of the present invention.

Best Modes for Carrying Out the Invention

Referring to Figure 8A, a computerized ECG analysis system provides an in-depth report of the results of the real-time monitoring of ambulatory patient ECG signals. The date for the report is derived from the patient's ECG signal. Each ECG waveform is analyzed and the results are retained in a small, lightweight ambulatory computer 10. At the conclusion of the monitoring period, the stored results are printed out in comprehensive report form by the companion desk-top unit 30.

The system comprises an Ambulatory Monitoring Unit (AMU) 10 and a Procedure Control System (PCS) 30 and 30a. The PCS 30 and 30a includes a Procedure Control Unit (PCU) 30 and a Procedure Report Printer (PRP) 30a. The AMU 10 is worn by the patient in a holster and the PCU 30 normally resides in the physician's office or laboratory. The printer 30a, functionally a part of the PCU 30, is physically a separate unit that is located closeby the PCU 30. The flow diagram of both data flow and control flow is illustrated in Figure 8B.

The ambulatory monitoring unit 10 is designed to monitor, analyze, and report on patient electrocardiogram signals taken from a modified lead electrode configuration. The monitoring is performed by a small, lightweight, ambulatory monitoring unit. The operation of the ambulatory

monitoring unit is normally initiated and shut down by the procedure control unit (PCU) 30.

The ambulatory monitoring unit or system is intended for use by qualified physicians. The reports that are produced as a result of an ambulatory monitoring procedure require interpretatio by a qualified physician. The electrocardiogram analysis performed by the ambulatory monitoring unit is designed to detect significant changes in rate, rhythm and/or shape of the patient QRS complexes. The QRS complex, an electrocardiogram wave pattern, is caused by ventricular depolarization. In addition, the analysis reports on the presence of a number of single beat anomolies, multibeat anomolies, heart rate ranges, S-T elevations and depressions, missed beats, asystole and patient activated symptomatic events.

The physician may require the patient to use the ambulatory monitoring unit along with a diary to record the patient's significant activities and symptoms. While useful for diagnosis, the diary is not required for proper ambulatory monitoring unit operation.

In the anticipated usage, the prescribing physician or paramedical personnel would:

a) Assure that the ambulatory monitoring unit contained fresh batteries.

b) Prepare the patient's skin and apply the electrodes.

c) Connect the leads to the electrodes.

d) Dock the ambulatory monitoring unit to the procedure control unit.

e) Initialize the ambulatory monitoring unit for the ambulatory procedure.

f) Insert the patient lead plug into the procedure control unit and visually inspect the electrocardiogram signal to assure good electrode placement and connection and proper gain setting.

g) Remove the ambulatory monitoring unit from the procedure control unit and place it in the holster.

h) Remove the patient lead plug from the procedure control unit and insert it into the ambulatory monitoring unit.

i) Attach the holster to the patient's clothing or body via the strap.

j) Instruct the patient as to ambulatory monitoring unit protection and care also the patient may be instructed on diary maintenance and physical activities.

k) Request that the patient return at a specified time for report generation, which may be after the 24 hours operating period or 72 hours under the data save period from the initiation time.

When the patient returns after the ambulatory monitoring period, the following activities would be performed:

a) Remove the ambulatory monitoring unit and holster from the patient.

b) Remove the patient plug from the ambulatory monitoring unit.

c) Insert the ambulatory monitoring unit into the procedure control unit and request a report.

During the ambulatory monitoring procedure, the operation of the ambulatory monitoring unit is directed by a control means that may be a hard wired control or a computer program which resides in the ambulatory monitoring unit memory. This control means, designated as the electrocardiogram monitoring and analysis means, receives input from the patient's electrocardiogram signals, from the ambulatory monitoring unit electronic components and from the patient event switch. These inputs are used to control the processing of ECG monitoring and analysis means. The results of the electrocardiogram analysis performed by ECG monitoring and analysis means in real time or ambulatory time are recorded in the ambulatory monitoring unit storage. It is this data that is used to construct the report that is generated for the physician at the end of the monitoring period.

ECG monitoring and analysis means, by analyzing the various inputs from the ambulatory monitoring unit components, can determine that the monitoring procedure must be terminated because of insufficient power. In this case the ECG monitoring and analysis means can place the ambulatory monitoring unit into a Data Save mode which

preserves the analysis data which has already been generated. Once placed in this state, the ECG monitoring and analysis means cannot be reactivated until the ambulatory monitoring unit is docked into the procedure control unit.

The electronics of the ambulatory monitoring unit are powered by small, commercially available batteries. These batteries will not be recharged but will be replaced for each long term monitoring procedure. The procedure control unit will test the batteries when the ambulatory monitoring unit is docked and will indicate when low power is detected.

The ambulatory monitoring unit provides certain indications to the patient and physician during the ambulatory period. It contains a time display for providing time correlation regarding events recorded by ECG monitoring and analysis means and the patient's diary if used. It provides an indication that the ECG monitoring and analysis means is detecting QRS complexes from the patient leads. It provides a patient event switch by which the patient can indicate that some symptom or event has occured that should be noted in the physicians report. Such events are noted at least by a time indication on the report. In addition, they also may be noted by recording the patient's ECG at the time that the event switch was depressed.

The ambulatory monitoring input generates an audio signal. It is used to indicate that the unit is going into the data saving mode and to indicate that significant noise or artifact or disconnected loads is preventing the ECG monitoring and analysis means from analyzing the ECG signals. The audio signal is not used to indicate any results of ECG analysis.

The ambulatory monitoring unit thus provides a vehicle for the ECG monitoring and analysis means while it performs the ECG analysis. The ambulatory monitoring unit provides the facilities for collecting and conditioning the ECG signal that is to be analyzed by the ECG monitoring and analysis means. The ambulatory monitoring unit provides the interface to direct patient in regard to input and time readout. The ambulatory monitoring unit provides an interface to the procedure control unit.

Referring now to Figures 1 and 2 of the ambulatory monitoring unit generally referred to by numeral 10 is a battery operated, 24 hour ambulatory heart monitor. The batteries in the block diagram of Figure 1 are shown as numeral 12. The ambulatory monitoring unit 10 monitors the patient's 14, shown in Figure 2, electrocardiogram activity via a single channel (two leads 16 and 18) connection employing a three patient lead that also includes a reference connection 20. The patient connector is illustrated by block 22 in Figure 1.

The AMU 10 is a portable, microcomputer-based device that detects the patient's ECG, classifies the QRS complexes individually and in sequence, then stores the results for subsequent generation of a summary report by the PCS 80. The ECG analysis is designed to detect significant changes in rate, regularity and/or shape of the QRS complexes. In general, the system devises a template of the patient's typical QRS complex. This complex is then used as a reference for recognition of QRS complexes. QRS complexes which do not match the reference complex are subjected to comprehensive shape analysis. Individual QRS shape, time position with respect to adjacent complexes and patterns of QRS shape and time position are used to identify atypical ECG phenomena. Atypical results are stored in memory on a priority-retention basis. Up to 30 types of single-beat changes and as many as 26 combinations of atypical cardiac occurrences are identified for reporting.

A simplified block diagram of the AMU is shown in Figures 1 and 2. Basically, the unit consists of an ECG amplifier 66, an analog-to-digital converter 68, a microcomputer 24, control logic 62 and a DC power source 34.

The ECG amplifier 66 includes two stages of amplification followed by a notch filter and a gain-programmable amplifier. This amplifier chain exhibits high common mode rejection and limits the input amplifier leakage current to the patient to less than 10 nanoampres. The notch filter suppresses pickup of the power line frequency.

The amplified ECG signal is sampled at regular intervals, converted to its digital equivalent and then placed in memory 26 all under the control of the AMU microprocessor 24. The operation of the microprocessor 24 is directed by a computer program, more fully explained hereafter, which resides in the AMU memory 50. This program examines the digitized ECG signals for rate, regularity and/or shape conformance. (A 10 second data examination cycle is used.) Atypical QRS complexes are retained in memory 26 on a priority classification basis; that is, complexes containing minor aberrations are automatically discarded in favor of those having more severe irregularities. It is this data, appropriately structured and formatted, which comprises the report that is generated for the physician at the end of the procedure.

The computer's input and output control logic 62 provides interfaces to the various auxiliary devices within the AMU such as the A/D converter 68, microprocessor 24, etc. This circuitry is used during AMU initialization to make a software-controlled adjustment of the ECG amplifier gain. It is also used during synchronization of the LCD time display 40, activation of the audible signal 44, mode control of the DC power source 34 and for general housekeeping routines. Additionally, the control logic 62 provides a patient interface 32 to allow the entering into memory 26 of Symptom switch depressions as identification of specific, patient-observed, physiologic discomfort periods.

The DC power source 12 consists of two 9-volt alkaline batteries connected in parallel. This power source 12 is capable of sustaining AMU operation during ECG monitoring and analysis for a minimum of 26 hours. Following the procedure period, the AMU power source 12 is able to preserve the results in memory for an additional period of 72 hours after battery "end-of-life" has been detected by the control logic 62; this is the data-save period.

Two, distinctively different audible signals are emitted to alert the user of an abnormal operating condition. For a low power warning, a continuous tone is sounded for five seconds. A disconnected patient lead or an excessive input noise condition is identified by an interrupted tones for a period of about 20 seconds. In the case of noise, the signal recurs at one minute intervals until the noise subsides. For a disconnected lead, the signal is not repeated.

Prior to use, the AMU 10 is initialized by inserting it into the "docking" receptacle of the Procedure Control Unit 30, discussed in more detail below. When the unit is docked, the timing/control interface 64 signals permit the orderly transfer of PCU program data into the AMU memory 26 for subsequent use during ambulatory operation. Also, at this time, the AMU power source 12 is checked under load and the LCD time display 40 is synchronized to the current time-of-day via a master timing reference contained in the PCU 30. As part of the "docking"

process, operation of the AMU 10 is automatically switched over from battery power to PCU power in order to conserve battery power.

Three chest electrodes 16, 18 and 20 connected to the PCU via a patient cable are used to sense the patient's ECG. The ECG signal is routed through an isolation amplifier in the PCU 30 before being applied to the AMU 10. This signal is shown as Analog Input in Figure 1.

At this point, the signal passes through the AMU ECG amplifier 66 where the proper programmable gain factor is introduced. Next, the ECG signals are digitized, entered into memory 26 and analyzed to determine the patient's typical (i.e., most common occurring) QRS complex. After selection, the typical QRS complex is routed back to the PCU 30 for inspection and approval by the physician. If accepted, the initialization process is completed; otherwise, the AMU 10 will discard the first selection and present its second choice as a typical QRS complex. This process is repeated until the physician is satisfied with the AMU's selection. Also as part of the initialization process, the name of the patient, time-of-day, date and the various system options selected are transferred into the AMU memory 26. Once the initialization process is completed, the AMU 10 is undocked from the PCU 30, the patient cable connections 16, 18 and 20 are transferred from the PCU 30 to the AMU 10 and ambulatory monitoring may begin.

The ambulatory monitoring unit 10 includes a digital microprocessing unit 24 and a 32 k byte random access memory 26. The microprocessing unit 24 (MPU 1802) continuously analyzes the patient's heart activity during the monitoring period of the patient 14. When the abnormal activity is detected, the MPU 24 stores data in memory relating to the detected abnormalities. The ambulatory monitoring unit 10 is docked at the end of the monitoring period in a procedure control unit through the procedural control unit connector 28. The procedure control unit (PCU) is illustrated by block 30 and referred to as the PCU. When the ambulatory monitoring unit 10 is connected to the procedural control unit (PCU) a visual and/or printed report is generated by the procedural control unit 30 that includes a CRT scope as well as a printer.

It should be noted that the patient 14 may alert to manual control the microprocessing unit 24 of the occurrence of an unusual event by depressing a event button 32 on the unit.

The ambulatory monitoring unit 10 may utilize two 9 volt transistor alkalized batteries for a full 24 hour procedure. Average battery life is expected to be 30 hours or more. A single battery may be installed for procedures requiring 12 hours or less. The batteries are illustrated by block, the power source 12 in Figure 1. The batteries are direct connected to the power supply unit 34 for controlling the output to the various systems and components withi the ambulatory monitoring unit 10.

It should be noted that the ambulatory monitoring unit may be as small as approximately a four inch by six and one half inches by one and one half inch rectangular volume. This ambulatory monitoring unit may weigh less than 24 ounces. All the electronic circuitry, memory, and power supply items are contained within this single envelope. The envelope is illustrated in Figure 2 by numeral 36. The case may be a seamless fiberglass tube with plastic end caps. One end of the cap may be defined as a front panel which houses the event button 32, a clock display 40 and the patient connector 22. The front panel or cap 42 include audio access to an audible alarm 44. The opposite end cap 46 illustrated in Figure 2 forms the rear panel and is removable to allow batteries to be changed. The rear panel houses the process control unit interface connector 28 which mates with the process control unit docking station 30.

Referring again to the block diagram in Figure 1, the controlling component is the 1802 microprocessing unit 24 which directly accesses all of the memory 26 and prom 50 through illustrated connection 52 connecting the microprocessing unit with the memory and prom. The prom 50 is acceptable only when the ambulatory monitoring unit is

docked into the process control unit 30 and automatically powered by the process control unit 30 with a fail safe system to be set forth in further detail herebelow. The microprocessing unit 24 communicates with the process control unit 54 (PCU) via programmed I/L using the data bus 56, the status bus 58, and the I/L address bus 60.

The control logic block 62 generates the indicated control signals are in command from the memory processing unit 24. It also communicates the ambulatory monitoring unit status via the status bus 58 to the microprocessing unit 24. The microprocessing unit disclosed herein may operate on a 4.096 MHZ clock 64 which results in a memory cycle time of 1.953 microseconds.

The microprocessing unit reads the personality prom 50 by issuing a series of input instructions with M4 to any mode 32 block of memory space. The least significant 5 bits of the address form the prom address for this instruction.

Referring now to Figure 4 the logic data board contains the ECG amplifier, the analog to digital converter, the direct memory access support logic, the digital gain control circuitry, the control byte for the purpose of setting the clock and controlling the gain. It also includes the one second timer and an alarm circuit to drive the sonic alarm unit.

The ECG amplifier consists of an instrumentation amplifier followed by a notch filter followed by a gain stage which is under digitial

gain control. This in turn feeds into an analog to digital converter. The front end of the instrumentation amplifier is composed of two sections of IC 1 feeding into a third section of IC 1. The signals from the patient leads can be found on P7, Pins 3, 4 and 5. Patient leads Pin 1 and 2 are shorted together in the connector to permit the microprocessor to sense the presence or absence of the patient lead connectors in the ambulatory unit. The diodes contained in DP 1 are intended to protect the system against any high voltage electrostatic discharges entering via the patient connector. Normally all of these diodes are back biased and not important to the system. The differential inputs of the instrumentation amplifier are returned to a reference voltage through RP 1, 3 megohm resistors and through R 1 and R 2 to the referenced voltage for the amplifier. P6, Pins 13 and 18 labeled L 1 and L2 also feed into the 2, 100 ohm resistors. This circuit is to permit an amplified and isolated ECG signal to be fed into the instrumentation amplifier when the ambulatory monitoring unit is docked in the physician's control unit. This permits the amplifier which is isolated by means of photo couplers to be mounted in the non-ambulatory portion of the equipment and thus relieve the ambulatory unit of this burden. The output of the instrumentation amplifier IC 1, Pin 10 is AC coupled into the next stage via capacitors C 2 and C 3. IC 2, Pin 1 feeds into the active twin T notch filter designed to be tuned to either 50 or 60 Hz. The tuning of this filter is controlled by

RP 4 potentiometers Pins 10, 12 and 14. RP 4 potentiometer Pin 16 is used to adjust the feedback into the active filter. RP 3, Pin 10, Pin 12 and Pin 14 are associated with the digital gain control. RP 3, Pin 6 and Pin 8 are tied into the digital switch IC 3 which permits either one or both of these points to open the amplifier gain control. RP 3, Pin 14 is set for the low gain setting of .04 millivolts per bit measured at the input leads of the patient connector. Full scale at the same point would be slightly over 10 millivolts. Full scale at the output of the amplifier would be approximately 1 volt. When gain 1 is shorted to V ref by the 4066, the amplifier gain is increased by a value of 2. When both gain 1, and gain 2 are shorted to the V ref, the amplifier is increased by a factor of 4.

Going back to the instrumentation amplifier, the last of the four operational amplifiers in IC 1 shown with inputs Pins 14 and 16 is used to boost the reference from approximately 1 volt to approximately 2 volts. At IC 2, Pin 14 the output of the gain control stage discussed previously has two resistors, R 13 and R 30, which are used to achieve a DC offset of approximately 100 millivolts. This will make it impossible for the output of the A to D converter to generate values of 00 through 07. These codes are reserved for control codes in the data stream. The A to D converter consists of Q 1, a constant current source feeding into C 6 which permits a linear ramp to be generated. When the output of IC 9 at Pin 14 is shut off, C 6 is permitted to charge at a linear rate. The comparator

IC 9, Pins 10 and 11 are used to determine when this linear ramp becomes equal to the analog voltage at IC 9, Pin 10. An eight bit counter at IC 7 clocked from TPA is started at the beginning of the ramp. The contents of this counter contains a value proportional to the value of the ramp at any particular time. The output of this counter is fed into an eight input gate, IC 8, to detect when the counter reaches full scale. The output of IC 8, Pin 13, then feeds through IC 15 and into IC 16 to generate the 4/8 millisecond timing for the A to D converter. When the 4/8 millisecond signal is low at Pin 8, IC 9, the output of IC 9, Pin 14 then permits the capacitor to start its linear ramp. When the linear ramp amplitude becomes equal to the amplitude of the analog signal at IC 9, Pin 10, Pin 13 will go high. This is coupled to Pin 6 of IC 12. The following leading edge of TPB then will cause Pin 2 of IC 12 to go low as this flip-flop becomes set. IC 14, Pin 6 will go high providing a clock for IC 5 and IC 6 on Pin 7. This clock causes the contents of the counter in IC 7 containing the digital value of the analog voltage to be transferred into the latches of IC 5 and IC 6. The clock also feeds Pin 13 of IC 12 and if "DMA-IN" at Pin 10 of IC 12 is true, this flip-flop of IC 12 will become set resulting in Pin 14 going low. Thus the signal "DMA-IN" is sent to the microprocessor requesting a DMA cycle. When the microprocessor responds, the DMA cycle is detected by IC 13 with a high on Pin 12 and Pin 13 resulting on a high on Pin 11 causing IC 12, Pin 12 to go high resetting this

flip-flop and causing IC 14 Pin 4 to go low which enables the digital value contained in IC 5 and IC 6 to be gated through the tri-state circuits to the data bus 0 through 7. The microprocessor in turn takes the data and transfers it to the memory at the location indicated by the DMA register. The counter in IC 7 continues to count until its output is all ones. This is detected by an eight input gate of IC 8 causing a low to occur at Pin 13 causing Pin 5 of IC 15 to go low which permits this flip-flop to be reset at the next TPB. This causes a high on Pin 2 of IC 15 which would cause a set to appear on Pin 7 of IC 12. This is necessary in case the analog signal is greater than full scale and coincidence was not detected by the comparator IC 9. In this case, IC 12 would call for a transfer of the full scale value of the counter IC 7 to IC 5 and IC 6. In any case, when the counter becomes full scale, IC 15 will be reset momentarily and then set again to generate a leading edge clock to Pin 10, IC 16 which will cause this counter to continue to advance.

After 256, 4 millisecond periods or 128, 8 millisecond periods, Q 11 of IC 16 goes positive furnishing the clock to IC 15 at Pin 11. This causes the interrupt flip-flop to become set with Q not Pin 12 going low to furnish an interrupt to the microprocessor. When the microprocessor responds to this interrupt request, State Code 0 and State Code 1 becomes high causing inputs 8 and 9 of IC 13 to become true causing Pin 10 of IC 13 to become high generating a reset to the interrupt flip-flop. C 20 at the output of IC 13 Pin 10

resolves the race condition on State Code 0 and 1 and insures that no spikes are generated at the output of IC 13.

Near the center of the page is IC 4 which contains six D type clocked flip-flops. These six latches contain various control states for the system. The latches are loaded from the data bus 0 through 5 by an I/O command "load control byte". "Load control byte" is clocked by TPB on IC 13, Pin 2. IC 13, Pin 3 then drives the clock signal into IC 4 loading the six control flip-flops.

The purpose of these flip-flops are as follows:

- Q 1 is enabled DMA
- Q 2 controls Gain 1
- Q 3 controls Gain 2
- Q 4, Q 5 and Q 6 have to do with the setting of the time of day clock display on the front of the ambulatory unit.

T 4 is also used to control the audible alarm shown at the lower center of the page. This alarm consists of a free running oscillator composed of and gate IC 13 and inverter IC 14. The oscillator runs at approximately 1 or 2 KHz and is enabled only when Pin 5 of IC 13 is high.

Just to the left of the circuit is IC 10 which includes a crystal oscillator and a count down circuit. The oscillator is at 35.795 KHz with a count down circuit of precisely one cycle per second at Pin 1. In order that this oscillator/counter operate Pin 8 must be high, which means that the flip-flop IC 11, Pin 2 must be reset. The microprocessor has a reset power up command used to power the ambulatory unit down in the event that the patient leads are disconnected. Thereafter,

at one second intervals, the one second time is used to clock IC 11 and cause the system to be powered up. Upon being powered up, the microprocessor will immediately determine if the patient connector leads have been plugged in. If not, the microprocessor will update the time of day by one second and power the unit down again. In the event that the microprocessor determines that the batteries are low, the unit will be powered down but with Q 6 of the control byte being set. This will cause the Pin 2, IC 4 to go low which will prevent the one second timer from firing again so that the unit will remain in the powered down or data save state until it has been returned to the PCU.

At the top center of the page is a resistor capacitor network connected to P 9 which is in turn fed by the event switch on the AMU panel. This feeds into a 47 MFD capacitor C 17 and to a divider network R 23 or R 26 and hence to external flag of the microprocessor. Since the microprocessor interrupt rate is approximately 1 per second, the capacitor is used to insure that if the switch is closed momentarily, the signal will last longer to insure that it has been sensed by the microprocessor. This concludes the discussion of the logic data board described on 300094.

Referring to Figure 5 which describes the logic of the microprocessor unit. On sheet 2 we have the microprocessor, the power control circuit and the I/O decoder circuit. On sheet 3 we have the memory interface logic. The microprocessor, IC 1, is an RCA 1802 microprocessor. It is

described in detail in the RCA manuals. The microprocessor operates with a 4.096 MHz cyrstal. This frequency was chosen to achieve a precise 250 samples per second of the EKG data. Just above the microprocessor is IC 2 of 7660. This circuit along with diodes D 1 and D 2 and capacitors C 3 and C 4 is used to achieve a very efficient (95%) voltage doubler circuit to drive Pin 40 of the 1802. This permits the operation of the 1802 at 4 MHz as opposed to only 2 MHz with the VDD set at 5 volts. The I/O circuitry of the 1802 still operates at 5 volts to be consistent with a remaining logic of the system. This is supplied by VL to Pin 16 of the 1802. At the center of the page, IC 9 is an 1853 decoder. This decoder looks at the N 0 signal, N 1 signal, and N 2 signal from the 1802 which are activated only during an I/O command. The three decoded outputs are "load control byte" Pin 10, "resent power up" Pin 11, and "PROM enabled" Pin 12. TBA at Pin 1 and TPB at Pin 15 are used to time the decode operation to insure spike free operation. At the top center of the page is the power control and regulation circuits for the system. VL is regulated at 5 volts but is under control of the power up flip-flop and may be switched on or off. VM is regulated by 5 volts but when the power is switched off, VM now regulates to 4 volts to insure that the data contained in the memory is not lost. The reference for the regulators is generated by D 7 a Zenner diode. The current for the Zenner is obtained from R 26. When "PW UP" is high, this feeds into Pin 11 of the comparator IC 12 and insures that

Pin 13 is cut off. The 339's have open collector output configurations. This permits the reference to feed through R 24 and R 25 into Pin 4 of the 339 with no attentuation. The regulator network consists of the 339 whose output is on Pin 2 and the transistor Q 1 and the choke L 2 of the feedback network at RP 2 and R 21 to form a switching regulator. When the voltage of VL drops slightly, Pin 5 will become slightly less negative than Pin 4. This causes the comparator whose output is on Pin 2 to conduct drawing current through R 20 and through the base of Q 1. This turns on Q 1 and causes a current flow from VB derived from the diodes D 5 or D 6 from either of the 9 volt batteries B 1 and B 2. When the voltage at VL rises sufficiently to cause the comparator to switch its output to high impedance state, the transistor Q 1 will turn off. The voltage across L 2 will rise in an attempt to maintain current flow through L 2. This causes the cathode of D 8 to go negative and the diode to conduct. Thus the energy stored in L 2 is effective in providing power into the load. This technique increases the efficiency of the power supply system over that of merely using a series regulator since the power of the full 9 volts is effective in generating power at the +5 volt level. When "PW UP" goes negative, the 339 whose output is at Pin 13 will conduct causing Pin 4 to go to 0 volts. This effectively turns off the regulator VL. However, the input to the VM regulator at Pin 8 is reduced by the network R 24, R 25 such that the VM regulator now regulates at 4

volts opposed to 5 volts which maintains the data save condition on the memory system.

The 339 (IC-12) whose output is on Pin 1 is used to detect low battery voltage. When Pin 6 becomes lower than Pin 7, the 339 output goes high indicating low battery voltage.

The connector P 1 contains the interface to the PCU. This interface is matted when the AMU is docked into the PCU.

This interface provides the following signals for communication with the PCU:

. DO-H thru D7-H	Data bus - by directional
. SC 0, SC 1	State codes direct from the 1802
. Q	A flip-flop output contained in the 1802
. TPA, TPB	Timing signals from the 1802
. N 0, N 1, N 2	I/O codes activated during I/O commands
. VM, VL	The output of the VM and VL regulators
. MRD-L, MWR-L	Memory read and memory write from the 1802
. AMU PR	AMU presence - used to detect when the AMU is docked
. V REF	Reference voltage from the logic data board
. V_B	Battery voltage after diodes D5 and D6

. B_1, B_2	Battery voltage direct from the positive terminal
. CLOCK	4.096 MHz clock
. L_1, L_2	Input points for the isolated ECG amplified signal used when docked
. 4 MS-H	4 MS timing signal from the logic data board
. AN OUT	The output of the ECG amplifier at the point of input to the ADC. This may be used for an input to the ADC for testing if a low impedance source is used..
. DMA-IN	To the 1802 for program load
. DMA-OUT	To the 1802 for testing
. WAIT-L, CLEAR-L	Control signals into the 1802
. INT-L	Interrupt to the 1802
. EF-1 thru EF-4	External flags into the 1802
. AUX SV	Power for the personality PROM
. GND	

In the AMU design specification, it is seen that the external flags have two definitions when the AMU is docked. Being docked is sensed by the state of EF-4.

External logic contained in the PCU drives EF-1, EF-2 and EF-3 when the signal Q-1. Q is contained in the 1802. Since EF-1, EF-2 and EF-3 have source impedances of 10K ohms, these are

easily overdriven by the circuits in the PCU.

Referring now to Figure 6 which shows the memory interface logic. The 1802 has only 8 lines for the 16 bit address. For each memory cycle the 1802 first transmits the high order 8 bits of the address over these 8 lines and then switches to the low order 8 bits for the remainder of the cycle. The AMU memory is 32,000 bytes. This is contained on two identical boards of 16,000 bytes each. Each memory board requires 14 address lines, A 0 through A 13. A 8 through A 13 is derived from IC 7 from memory address lines 0 through 5. This is clocked in by TBA. The lower address bits to the memory LA 0 through LA 7 and HA 0 through HA 7 are passively driven by IC 5, IC 6 and IC 8.

It should be noted that IC 4, IC 5, IC 6, IC 7 and IC 8 are all powered by VM. This is to insure that control of the address lines is not lost when power is switched off. This is necessary to assure minimum standby current in the memory system. The network at the top left hand corner of the drawing controls the timing of the power on and off sequence. When "PW UP" becomes high, the WAIT-L immediately becomes high. "PW UP" high also feeds through the 100K resistor R 14 into a 0.22 MFD capacitor, C 12, to generate a delay of approximately 20 milliseconds. The output of this capacitor feeds into the Schmidt like circuit consistent of two 4049 inverters such that when the threshold of this circuit is reached, the circuit is rapidly switched to the high state at Pin 12 of IC 11. This permits CLEAR-L to become

high when both WAIT-L and CLEAR-L are high, the microprocessor is permitted to run. When "PW UP" goes low as a result of a microprocessor command, the signal WAIT-L immediately goes low which immediately halts the microprocessor. A timing network to the left driven by TPA and TPB is designed to generate a signal at IC 10, Pin 10 commencing at the trailing edge of TPA and extending to the trailing edge of TPB. The output of this signal is fed into G1 of the decoder IC 4. Delay power up of the Schmidt trigger just discussed also feeds into Pin 7 to enable the decoder in IC 4. "PW UP" directly feeds into Pin 6, the same decoder to assure disabling this decoder immediately when "PW UP" goes false. The decoder looks at MA 6 and MA 7 on Pins 3 and 4 respectively. Output of the decoder HE-L or LE-L is used to select one or the other of the two memory banks. The resistor network, RP 1, is used to terminate the address line to the ground state when VL is reduced to 0 volts to assure that the input to the IC 4, 5, 6 and 8 are not indeterminate. IC 3 contains a personality PROM for the ambulatory unit. The personality PROM is powered when the ambulatory unit is docked into the physician control unit. When IC 3 does not have any power, its outputs on Pin 1 through Pin 9 is in the high impedance state and will not load the data bus. When IC 3 does have power (+5 volts on Pin 16) it will still be in the high impedance state so long as CS Pin 15 is high. The I/O command "PROM EN" from the I/O decoder discussed earlier will drive Pin 14 of IC 2 high resulting in a low at Pin 15 generating

chip select low at Pin 15, IC 3 enabling the output of the personality PROM to drive the data bus. The address to dervice the PROM is the low order address bits LA 0 through LA 4.

The 3 inverters of IC 11 at the top of the page are unused and their inputs are grounded. R 10, the 100K resistor, connected Pin 16 of IC 3 to ground is to insure that Pin 16 remains at ground when +5 V-AUX is in the open position when the device is ambulatory.

We will now direct our attention to the logic of the 16K memory board, Figure 7.

At the center of this drawing is a matrix of 4 x 8 ICs that make up the 16K bytes of memory. Each IC is configured as a LK x 4. Thus a pair of ICs represents a 1K x 8 or 1K bytes of memory. There are 16 such pairs on each memory module. To activate any one pair requires one of the signals ENBK 0 through ENBK 15 generated by IC 33 and IC 34. These ICs are decoders of the address lines A 10, A 11, A 12 and A 13. The signal on P 5, Pin 17, "XE-L" indicates that this corresponds to either LE-L for the low order bank or HE-L for the high order bank. This is required to activate either IC 33 or IC 34 at Pin 7. It is also necessary to activate IC 32, Pin 5 along with memory read Pin 4 to cause a high at IC 32 Pin 6 which in turn causes a low at IC 32, Pin 3 to enable the bus transceivers IC 31 and IC 30. At P 5, pin 20, we have the signal MWR-L from the microprocessor which feeds MWR into all of the memory IC chips and also feeds MWR into Pin 7 of IC 30 and IC 31 which is necessary to reverse the

direction of the transceivers to drive data from the bus into the memory elements.

The diode at the lower left hand portion of the drawing provides an "AMU" function of MRD-L and MWR-L to feed into Pin 8 of the decoders IC 33 and IC 34.

Referring now to the microprocessing unit 24, its I/O functions are:

N	OUTPUT	INPUT
1	Spare	Spare
2	Spare	Resent Output Ready
3	Spare	Spare
4	Enable PROM	Enable PROM
5	Resent Power Up*	Reset Power Up
6	Load Control Byte	Invalid
7	Write PCU data	Read PCU Data

*Enable time set (control bit 5) transferred to Data Save.

The control byte is defined as follows:

BIT	FUNCTION
0	ENABLE DMA-IN
1	GAIN 1
2	GAIN 2/Increment minutes*
3	ALARM ON
4	MUSIC SYMBOL ON/Increment hours*
5	ENABLE TIME SET/Data save

*When ENABLE TIME SET (Bit 5) is true these bits increment time. When bit 5 is false the alternate function prevails.

Microprocessing unit status:

FLAG	Q=0 OR AMBULATORY	Q=1 (AND DOCKED)
EF-1	Patient connected	Message
EF-2	Event	Input Ready
EF-3	Battery OK	Output Ready
EF-4	Docked	Docked

Referring to the ambulatory monitoring unit memory 26 may consist of 64 1Kx4 CMOS chips organized in a 32K x 8 array. This configuration minimizes power consumption in that only two chips are active at any one time. Power consumption is further reduced by lowering the chip power level to +3 volts in the standby mode as set forth below.

The electrocardiogram (ECG) signal processing system receives analog signal from the patient 14 Figure 2 and forwards this signal to the linear amplifier 66 shown in Figure 1 through the patient connector. The amplifier 66 having four gain levels set under program control. Recovery time from a gain adjustment is less than 100 milliseconds. The gain levels are controlled by device control bits as follows:

CONTROL 2	BIT 3	GAIN LEVEL
0	0	25 ADC Channels/MV (1/2 normal)
0	1	50 ADC Channels/MV (normal)
1	0	100 ADC Channels/MV (2X normal)
1	1	125 ADC Channels/MV (approximate)

The amplifier 3db bandpass is from .32 to 30 or 40HZ depending on whether the notch filter is set for 50 or 60 HZ.

The A/D converter 68 is connected to the amplifier 66. The A/D converter employes a 500 microsecond ramp and generates an 8 bit sample every 4 or 8 ms (strapping option). The first 8 channels of the 256 available in the 8 bit sample are not used by the A/D convertor. Sample values 00 to 07 are not generated by the hardware and are

reserved for system use. The samples are loaded into memory via DMA transfer and an interrupt is generated within 500 microseconds after the 128th or 256th sample. Figure 3 illustrates the interrupt timing.

The connection of the patient leads is sensed by a shorting jumper in the connector which drives EF-1 in the MPU when Q=O.

The audible alarm 44 is driven by device control bit 1. Whenever the bit is on a continuous 400 HZ tone is sounded.

The time display 40 contains a watch chip, 12 hour LCD display with AM/PM and musical symbol indicators and a self contained crystal controlled clock oscillator (accuracy within 30 seconds/24 hours). Bit 4 of the device control byte controls the music symbol. Bit 5 enables time setting and the stops the display clock. While the bit is high, the MPU can increment hours or increment minutes via control bits 4 and 3 respectively. When bit 5 is turned off, time resumes at zero seconds. The clock is powered whenever the ambulatory monitoring unit is not in the "Data Save" condition. Removing power, by entering Data Save signal and restoring will reset the time to 12:00 (midnight). Power must be removed for 100MS and applied for 100MS before time may be set. Since entering "Data Save" would normally power the ambulatory monitoring unit down, this function must be performed only while the unit is docketed and the PCU is overriding the power down. This is set forth in further detail hereinbelow.

The "EVENT" button is sensed by the MPU via EF-2 when Q=0. The program must test the flag at least once each second to insure that a depression is not missed.

The ambulatory monitoring unit is power by two 9 volt "transistor" batteries 12 connected in parallel and isolated by diodes. The diodes protect against damage caused by temporary reversal of polarity when the battery is installed.

While the ambulatory monitoring unit is functioning normally, the battery drain is approximatel 25 MA. This results in a life of about 15 hours per battery for a total of 30 hours.

The ambulatory monitoring unit can under program control power down all its control electronics including the MPU and reduce the memory voltage to 3 volts. The only functions remaining active are the time display and a one second wake up timer. This reduces the battery drain to about 2.5MA. At this level, battery life is increased by a factor of ten and in addition, memory data will be retained for fifty hours after the batteries have dropped to the five volt level. The MPU program powers down by issuing a "Reset Power Up" (RPU) function. The effect of RPU is modified by the state of control bit 5. If control bit 5 is true, the power down is permanent and power is not restored until the AMU is docked. If control bit is false, power is restored and the MPU restarted once each second. The former is called the "Data Save" and the latter the "Leadless" condition since it is normally invoked whenever the patient leads have been disconnected.

Battery status is passed to the MPU on EF-4 with Q=O. The flag is normally true and go false when the battery has dropped to 5 volts. Below this level, MPU operation becomes unreliable and the program must enter the "Data Save" condition within ten minutes.

The personality PROM is a high current device and hence is powered by the PCU only. The 5 volt auxiliary power line 1 supplies power to the PROM and also overrides the "Leadless" or "Data Save" conditions in the AMU.

When batteries are first installed in the AMU, power remains shut off and the AMU is in the "Inactive state." The AMU is activated by the PCU after a battery test is performed.

The ambulatory monitoring unit communicates with the procedure control unit via a 41 pin connector. Ambulatory monitoring unit/procedure control unit is as follows:

SIGNAL NAME	MNEMONIC	SIGNAL TYPE	SOURCE AMU	SOURCE PCU
Data Bus 0	DB-OH	CMOS	X	X
Data Bus 1	DB-1H	CMOS	X	X
Data Bus 2	DB-2H	CMOS	X	X
Data Bus 3	DB-3H	CMOS	X	X
Data Bus 4	DB-4H	CMOS	X	X
Data Bus 5	DB-5H	CMOS	X	X
Data Bus 6	DB-6H	CMOS	X	X
Data Bus 7	DB-7H	CMOS	X	X
Interrupt	INT-L	CMOS		X
External Flag-1	EF-1L	CMOS		X
External Flag-2	EF-2L	CMOS		X
External Flag-3	EF-3L	CMOS		X
External Flag-4	EF-4L	CMOS		X
N Register O	NO-H	CMOS	X	
N Register 1	N1-H	CMOS	X	
N Register 2	N2-H	CMOS	X	
State Code 0	SCO-H	CMOS	X	
State Code 1	SC1-H	CMOS	X	

SIGNAL NAME	MNEMONIC	SIGNAL TYPE	SOURCE AMU	SOURCE PCU
4 Millisecond	4MS-H	CMOS	X	
Q	QH	CMOS	X	
WAIT	WAIT-L	CMOS		X
CLEAR	CLEAR-L	CMOS		X
DMA IN	DMA-IN-L	CMOS		X
Timing Pulse B	TPB-H	CMOS	X	
Memory Read	MRD-L	CMOS	X	
AMU Present	AMUP-L	CMOS	X	
*DMA OUT	DMA-OUT-L	CMOS	X	
*Memory Write	MWR-L	CMOS	X	
*Timing Pulse A	TPA-H	CMOS	X	
*System Clock	CLK-H	CMOS	X	
Lead-1	Lead-1A	ANALOG		X
Lead-2	Lead-2A	ANALOG		X
Analog Out	AOUT-A	ANALOG	X	
Battery Voltage-1	VB-1	POWER	X	
Battery Voltage-2	VB-2	POWER	X	
Battery Voltage	VB	POWER	X	
Memory Voltage	VM	POWER	X	
Logic Voltage	VL	POWER	X	
Auxil. 5 Volts	5V-AUX	POWER		X
Ground	GND	POWER	X	X

*These signals are not used by the procedure control unit and are used for test only.

The electrical characteristics of the unit include that all digital signals are 5 volt CMOS levels. The PCU holds all I/O lines in a high impedance state until the AMU is locked in place and powered up at the docking station. The maximum loading is 100K ohm and 20 pf regardless of whether the PCU is powered up or not. The data bus lines are pulled up with 22K resistors to +5 volts in the PCU.

In docking the ambulatory monitoring unit the following should be noted. The presence of an ambulatory monitoring unit at the PCU docking station is sensed electrically through the interface connector. The PCU program then actuates a mechanical

latch which locks the AMU in place and sets "Docked" status to the AMU. The patient connector must be physically disconnected before the PCU interface connector can be mated. Patient monitoring while docked is accomplished by plugging the patient leads into the patient connector on the PCU. The EKG signal is passed through an isolation amplifier to the AMU/PCU interface connector and into the AMU input terminals. The isolation amplifier is relatively wide band and linear so as to preserve the integrity of the patient ECG signal. In addition, it is optically coupled to insure a maximum of 10 microamperes leakage at the patient connection. The amplifier has a gain of 250 which is compensated for by an attenuation of the same amount in the AMU. The docked condition is entered from the "Leadless", "Data Save" or "Inactive" conditions. The AMU "Inactive" state is detected by the PCU hardware by sensing VM < 1 volt. The "Data Save" condition is not sensed by the PCU hardware.

There is power control in the AMU. An inactive AMU docked at the PCU is first checked for battery condition. This is done under PCU program control by applying a current pulse to each battery while monitoring output voltage. The PCU activates an inactive AMU by driving Vm to 5 volts for 100ms. This is followed by a load sequence. The PCU supplies power to the AMU during all the time it is docked. This insures against loss of data in a low battery situation. The "Data Save" or "Leadless" condition in the AMU is overridden by application of 5 volt auxiliary power from the PCU. The PCU first monitors Vm to insure that the AMU is powered

down (VM < 4 volts) and then applies 5 volt aux. power. A power failure in the PCU causes the AMU to be ejected. If a "Data Save" condition existed prior to docking, the AMU reverts to that state. When power is restored, the AMU may be redocked without loss of data. The "Data Save" condition is controlled by AMU program command only and requires initialization by the program on power up. This must be done while the unit is docked in the PCU.

The PCU initiates the load sequence by asserting "CLEAR". This signal forces any acitivity in the AMU to an abrupt halt by resetting the MPU. While holding "CLEAR" true, the PCU initiates its output DMA channel and asserts "WAIT" to the AMU forcing the MPU into the load mode. The PCU interface hardware completes the DMA to DMA transfer. The PCU program then releases "WAIT" and after 10 microseconds releases "CLEAR". AMU program execution is initiated starting at memory location zero as soon as "CLEAR" is released.

AMU output is DMA controlled in the PCU and programmed I/O in the AMU. The DMA priority is sufficiently high to insure that when the AMU inputs data at its maximum rate of 125K bytes/sec, no data will be lost. A transfer is initiated by the PCU raising the "Message" signal which at the next rising edge of the 4 ms signal interrupts the AMU. The AMU uses the "Message" flag to determine the source of interrupt and the "Input Ready" flag to determine end of message.

The PCU drops "Message" after the first byte is transferred. "Input Ready" is dropped after each byte transfer and is raised within 6 microseconds to insure continuity of transfer. When the last byte has been transferred, "Input Ready" stays low (100 microseconds minimum), the AMU program senses the low condition and terminates the input sequence.

AMU output is via an independent DMA channel in the PCU and program controlled in the AMU. The PCU DMA channel is capable of supporting a 125K byte/second transfer rate. The "Output Ready" flag indicates that the PCU DMA channel is armed and ready to accept output from the AMU. This flag is sensed by the AMU prior to initiating an output sequence. The AMU issues consecutive output commands until the entire block has been transferred. It then sends "Outputs Complete" which resets the "Output Ready" flag terminating the sequence. If the AMU attempts to send a longer block than the PCU DMA channel has been set up for, the additional data will be lost.

While the AMU is docked, the PCU continuously monitors AMU DMA activity. All data transferred from the A/D converter is captured by the PCU interface hardware and transferred to the PCU under program control.

The AMU personality PROM is powered by the PCU via the 4 volt auxiliary power input. The PROM is read by the AMU/MPU after power has been supplied.

PCU program control/status bits.

CONTROL PIO	STATUS
A0. Test Batteries	O. AMU-1 present
A1. Lock AMU1	1. AMU-2 present
A2. Lock AMU2	2. A/D Converter EOC
A3. Activate AMU	3. Message Ready Latch*
A4. CLEAR	4. Output Ready Latch**
A5. WAIT	5. Undefined
A6. +5v AUX	6. Undefined
A7. Undefined	7. Undefined

B0-B7	AMU DATA
BSTB	DMA Byte captured **
ASTB	Output Ready Latch, interrupt input

* PCU output function
** PCU input function

Additional functional specification of the ambulatory monitoring unit are as follows:

PERFORMANCE AND CAPACITY SPECIFICATIONS

ECG RATE RANGES

The AMU will detect QRS complexes and classify individual complexes and sequences of QRS complexes.

ECG DETECTION RANGE

The AMU will detect QRS complexes at rates of up to 300 per minute.

ECG CLASSIFICATION RANGE

The AMU will classify the detected QRS complexes which occur in the range of 15 to 190 per minute.

AMBULATORY POWER SOURCE

The AMU is required to operate for long periods of time powered only by its self-contained power source. This power source must be able to sustain the full processing load of the AMU during an operating period and must also be able to maintain the stored data and programs during a "data-save" period.

OPERATING PERIOD

The AMU ambulatory power source will be capable of sustaining the AMU during the ECG monitoring and analysis operations for at least 24 hours.

DATA SAVE PERIOD

Following the Operating Period, the ambulatory power source will be able to preserve the programs and data then contained in the volatile storage of the AMU for a period of 72 hours.

MODES OF OPERATION

The AMU has 6 different states or modes. These modes are named:

1. Powerless
2. Inactive
3. Docked
4. Armed
5. Operational
6. Data Save
7. Diagnostic

These modes are described in the following sections.

Powerless mode

This mode exists during the time period when the batteries are not in the AMU or during the period when the power level of the batteries is too low to maintain the data storage. Exit from this mode occurs when new batteries are put into the unit. The AMU then enters the Inactive mode.

Inactive mode

This mode exists from the time fresh batteries are inserted into the AMU until the AMU enters the Docked mode.

Docked mode

This mode exists during the period when the AMU is mated with the PCU (procedure control unit.) During this mode the AMU may:

1. Be initialized with software
2. Be tested in a diagnostic manner
3. Have its data copied into the PCU
4. Have its personality data read
5. Return AMU to inactive mode.

The AMU normally enters the Armed mode next.

Armed mode

This mode exists when the unit has a software load and adequate power and no leads inserted and is not docked. During this mode, the time of day is maintained in the visual display and the processor maintains the internal processor time during brief periods of activation. Such periods are triggered by external hardware signals at one (1) second intervals. From this mode the AMU can enter, the Docked mode, the Operational mode, or the Data Save mode.

Operational mode

This mode is entered only from the Armed mode. During this mode the AMU analyzes QRS's. The mode is entered when the leads are inserted into the AMU in the Armed mode and the low power indication is not on. From this mode the AMU can enter the Armed mode and the Data Save mode.

Data Save mode

This mode is entered from the Armed mode or the Operational mode when the low power indication is sensed. Before this mode is entered, a storage ceck sum is computed and stored. In this mode, minimal power is used for maintaining the contents of memory. The AMU will enter the Docked mode next.

Diagnostic mode

ECG DATA ACQUISITION FUNCTION

SAMPLED DATA PRECISION

The AMU will sample the patient's ECG at a specified rate and produce a digitized representation of the ECG value.

ECG SAMPLING RATE

The ECG will be sampled at a rate of 250 samples per second or .004 seconds between samples. The precision of the sample period will be +-.05%.

ECG SAMPLED VALUES

The ECG signal sample will be converted into a digital format. The digitized sample will consist of values in the range 4 to 255. These values will be formatted into an 8 bit representation.

The AMU will have three sensitivity levels for ECG sample conversion. (These sensitivity levels are related to medical standards for ECG display.)

These sensitivity levels are defined as follows:

LEVEL	UNIT VALUE OF CONVERTED SIGNAL (MILLIVOLTS)	VOLTAGE RANGE (MILLIVOLTS)	ECG DISPLAY (MILLIVOLTS MILLIMETER
HIGH	.01	+-1.25	.05
MEDIUM	.02	+-2.5	.1
LOW	.04	+-5.0	.2

For all sensitivity levels, ECG voltage of zero is converted to the sample value of 12.8.

ECG ANALYSIS FUNCTIONS

ECG DEFINITIONS

QRS COMPLEX

The QRS complex is that variation of the ECG signal which is generated by atrial and ventricular depolarizations. The R point is the point within the QRS complex associated with the maximum excursion of the signal from the baseline.

QRS RATE

The QRS rate is a measure of the number of QRS complexes per unit time. By definition, the QRS rate is measured in units of beat per minute. The rate is computed via the following formula:

60,000 x (1/arithmetic mean of 8 QQ intervals).

QRS REGULARITY

Regularity is a measure of the constancy of pattern of the QRS coupling interval. Regularity is calculated for a single QRS complex as the number of matches of the coupling interval with the eight preceeding 8 couple intervals. Two coupling intervals are said to match if they differ by not more than +-12.5%.

MAJOR EVENTS

Significant changes in rate, rhythm or shape

Rate: increase or decrease in qrs frequency
Rhythm: increase or decrease in qrs regularity
Shape: increase or decrease in qrs shape

ECG CONDITIONS

RATE CLASSICIATIONS: Sinus Rhythm

0 - 25 bpm
25 - 40 bpm
40 - 50 bpm
50 - 60 bpm
60 -100 bpm
100 -150 bpm
150 -190 bpm
190 - up bpm

SINGLE COMPLEX EVENTS

SINGLE QRS ANOMALY CLASSICIATIONS

Abtrial: premature - = 6 per minute, 6 per min.
Aberrant/Fusion - = 6 per minute, 6 per min.
Ventricular: premature - = 6 per minuee, 6 per min.

MULTI COMPLEX EVENTS

MULTI-QRS ANOMALY CLASSIFICATIONS

Bigeminy - Atrial, Ventricular
Couplets - Ventricular
Triplets - Ventricular

BLOCK CLASSIFICATIONS

Single missed beat
Multiple missed beats
Escape beat

S-T EVENTS

PRIORITIES OF ECG ANOMALIES

The priorities of the ECG events are listed below.

FIDUCIAL POINT

The fiducial point for a QRS complex is the sample point on the Q-R slope at which the first difference of the data values achieves the maximum.

PATIENT INTERFACE FUNCTIONS

The functions of the AMU which are accessible by the patient are described in this section.

TIME DISPLAY FUNCTION

The AMU will display the time of day in hours and minutes.

The time display consists of hours, minutes and an "am" or "pm" indication.

The time of day is set during the Docked mode when the AMU is initialized. The time of day display will be maintained until the AMU goes into the Data Save mode or the Powerless mode.

The time of day is independent of the processor maintained time and is not expected to differ from it by more than 1-minute in 24 hours.

OPERATING INDICATION FUNCTION

The AMU will provide a visual indication that QRS detection is occuring in this operational indication is a symbol which is illuminated at approximately 50% duty cycle as long as the software is detecting QRS complexes.

SIGNAL CONDITION WARNING FUNCTION

The AMU will generate an audio signal in the presence of noise or artifact or disconnected leads in the Operational mode which persists for more than

1 minute. The signal will be toggeled with a 50% duty cycle at a cycle period of not more than 4 seconds. The togelling will continue until one of the following occurs:

- . the artifact subsides
- . the AMU enters the Armed mode
- . the AMU enters the Data Save mode
- . the AMU enters the Powerless mode

LOW POWER WARNING FUNCTION

The AMU will generate an audio signal when the Data Save mode is about to be entered. This warning signal is a continuous tone and is sounded for five (5) seconds.

SYMPTOMATIC REQUEST FUNCTION

The symptomatic request function is activated by an event switch. This switch is activated by depressing it. It is deactivated when the pressure is released. The software senses both the activation and deactivation of the switch. The processing which is associated with the event switch may be enabled or disabled during initialization in the Docked mode.

If enabled, the software sensing of the activation initiates an "event period". The time of the initiation of the event period is logged in the AMU storage. The AMU will be capable of storing fifty (50) such time marks.

The physician can elect to have snapshots taken as a result of switch activation. There are mutually exclusive techniques that are options to the physician: imperative snapshot generation and conditional snapshot generation.

The imperative snapshot generation technique will cause a snapshot to be generated for each event period which the patient initiates. The snapshot generated will be labeled as a symptomatic event. The actual time period covered by the snapshot is determined as follows:

A. In case the AMU algorithms determined that:

* a snapshot should be taken of data being analyzed when the event period is initiated

Or

* a snapshot has been recorded by the algorithms during the last 10 seconds

Then that snapshot is also labeled as a symptomatic event and given the higher of its original priority or the manual event priority. In case the patient initiates another event period within 10 seconds, no snapshot will be recorded.

B. In case the algorithms do not detect any ECG events that should be recorded in a snapshot from the current data then a snapshot will be taken that is centered in time approximately five (5) seconds prior to the event period initiation. In case the patient initiates another event period within 10 seconds of the previous period, then the snap from the previous period will not be kept if it was also generated by this condition (i.e. Case B.) the physician may specify the maximum number of snapshots that can be recorded in this case. The default number is five (5). In case more than the maximum number are requested then the chronologically newest snapshot is discarded.

The conditional snapshot generation causes a snapshot to be taken only in the case when the AMU algorithms determine that a snapshot should be recorded during the event period or the 5 seconds which preceed the event period. Any such snapshot would be labeled as a symptomatic event and given the higher of the two priorities.

It should be noted that the preferred embodiment of the AMU circuitry is set forth herein below.

The PCS (see Figure 8) is a desk-top, miniaturized computer system consisting of a keyboard/display device 30 and a separate graphics-quality printer 30a. Both devices are powered directly from a standard ac power source and employ individual switches to control the application of power.

The keyboard/display device 30 contains the microcomputer and provides a receptacle (or port) for "docking" the Ambulatory Monitoring Unit. In addition, this device displays service lists which prompt the operator in the use of the system. The keyboard provides a means by which the operator communicates with the computer. The graphics-quality printer supplies a hard copy report of the results of the ambulatory procedure.

The main functional elements of the PCS are shown in Figure 9. For patient safety, during AMU initialization, the patient's ECG signal is passed through an isolation amplifier 82 contained in the AMU analog interface section 80. The buffered ECG signal is routed from the patient through the PCU docking receptacle 84 and to the AMU 10 where it is digitized.

The AMU digital interface 80 includes line drivers and receivers which buffer the signals to and from the AMU during the reporting phase of the AMU and the loading of software instructions. Additionally, the interface 80 permits monitoring of the AMU battery status and the application of

PCU power to operate the AMU during docking. Also included in the PCU is a solenoid (see Figure 17) which releases the AMU from the "docked" position. Upon user request, this solenoid can be energized forcing the AMU away from the docking receptacle and allowing the unit to be manually withdrawn by the user.

The buffered, digital AMU signals are interfaced with the PCU system bus by the I/O logic 86. This section controls the transfer of the contents of the AMU 10, the ECG analysis program, and the system diagnostics to and from the PCU.

The program memory consists of EPROMs (See Figures 10 and 10a) which contain the resident program used during ECG analysis as well as display related programs which "prompt" the operator in the use of the system.

When power is first supplied to the PCU, basic test routines are activated to briefly check the main components of the system. System diagnostics 96 contained in an auxiliary EPROM module permit a thorough test of the system as well as providing fault location for module replacement. An LED display 98, together with CRT diagnostic error messages, assist in localizing the problem to a specific area.

The keyboard section includes alphanumeric and function keys which permit the user to select specific services, enter patient/physician data, make procedure annotations, edit test results, modify test routines, etc. The keyboard entries are decoded and the associated request/commands are routed to the appropriate device via the system bus.

The patient's summary report is printed out on the electrosensitive, graphics-quality printer 30a. A complete page is printed in approximately 10 seconds. Two horizontal dot resolutions are employed during the printing cycle. The lower resolution is used for the alphanumerics and the higher density is necessary for graphics reproduction.

The printing cycle can be started and stopped at the end of the page via a keyboard entry; however, paper feed, character/graphics printing and paper cutting are all controlled automatically by the program.

The data displayed on the CRT monitor is derived from three separate memories: graphics 88, grid 90 and alphanumerics 92. The contents of these memories are read out and summed in a video driver stage 94 before being applied to the raster-scan monitor. The monitor presents the user service-selection menus and provides a high resolution display of static and dynamic ECG data. For a static display, either a grid or calipers can be superimposed on the ECG waveform to assist in the analysis of the data; also, the displayed data can be expanded for closer observation.

Referring to Figures 10 and 10a, the central processing unit 100 is a Z-80 based system using a memory translation ram 102 to extend the Logical 65K of addressing space to 1M (20 bits). The 256 words of address translation ram are addressed by the upper 7 bits of the Z-80 address bus and a 1 bit offset register. This results in up to 2

memory maps which can be selected by I/O commands to the memory map register.

The 8-bit data bus is bi-directional, and buffered between all boards. The DMA channel will be implemented with LSI logic, sharing the data and address busses with the CPU 100.

The CRT display is actually derived from three sources. Two are bit by bit binary graphics 88; the 64K x 8 stores up to four EKG traces, while the Lk x 8 contains the grid 90 and caliper matrix. The third block of dedicated dual-port memory contains ASCII character strings, to be formatted into video by the alpha-numeric video generator 92.

The rest of the I/O 104 is primarily interrupt driven, with the printer-plotter and disc control being DMA as well.

The system electronics is defined as follows:

Pin	Mnemonic	*	Source	Description
1	VCC	U	PS	+5 volts
2	VCC	U	PS	+5 volts
3	IEIOH	U	Bd	Interrupt Enable IN 0
4	IEOOH	U	Bd	Interrupt Enable OUT 0
5	IEI1H	U	Bd	Interrupt Enable IN 1
6	IEO1H	U	Bd	Interrupt Enable OUT 1
7	IEI2H	U	Bd	Interrupt Enable IN 2
8	IEO2H	U	Bd	Interrupt Enable OUT 2
9	IEI3H	U	Bd	Interrupt Enable IN 3

	10	IEO3H	U	Bd	Interrupt Enable OUT 3
	11	INTL	U	Any	Maskable Interrupt Req
5	12	NMIL	U	PS	Non-maskable interrupt Req
	13	SYSRESH	U	CPU	System Reset, active high
	14	SYSRESL	U	I/O	System Reset,
10				CPU	active low
	15	GND	U	PS	Power supply return
	16	GND	U	PS	Power supply return
	17	DMAREQAH	U	I/O	DMA REQ, Channel A
15	18	DMAACKAL	U	CPU	DMA Acknowledge, channel A
	19	DMAREQBH	U	I/O	DMA REQ, channel B
	20	DMAACKBL	U	CPU	DMA Acknowledge, channel B
20	21	DMAREQCH	U	-	DMA REQ, channel C
	22	DMAACKCL	U	CPU	DMA Acknowledge, channel C
	23	DMAREQDH	U	-	DMA REQ, channel D
	24	DMAACKDL	U	CPU	DMA Acknowledge,
25					channel D
	25	DMAIORDL	T	CPU	DMA IORD in process
	26	DMAIOWRL	T	CPU	DMA IOWR in process
	27	DMA1EOP1	T	CPU	DMA chip 1 EOP signal
	28	DMA3EOPL	T	CPU	DMA chip 2 EOP signal
30	29	undefined	T		
	30	undefined	T		
	31	undefined	T		
	32	undefined	T		
	33	GND	T	PS	Power supply return
35	34	GND	T	PS	Power supply return
	35	IORQ3XL	T	CPU	IO Request, address 30-3F
	36	IORQ4XL	T	CPU	IO Request, address 40-4F
40	37	IORQ5XL	T	CPU	IO Request, address 50-5F
	38	IORQ6XL	T	CPU	IO Request, address 60-6F.

	39	IORQ7XL	T	CPU	IO Request, address 70-7F
	40	DB0H	T	All	System Data Bus 0
	41	DB1H	T	All	System Data Bus 1
5	42	DB2H	T	All	System Data Bus 2
	43	DB3H	T	All	System Data Bus 3
	44	DB4H	T	All	System Data Bus 4
	45	DB5H	T	All	System Data Bus 5
	46	DB6H	T	All	System Data Bus 6
10	47	DB7H	T	All	System Data Bus 7
	48	IORQL	T	CPU	System IO Request
	49	GND	T	PS	Power supply return
	50	GND	T	PS	Power supply return
	51	MREQL	T	CPU	Memory Request
15	52	RDL	T	CPU	Read
	53	WRL	T	CPU	Write
	54	RFSHL	T	CPU	Refresh
	55	BUSAKL	T	CPU	Bus Acknowledge (DMA in process)
20	56	HALTL	T	CPU	MPU Halted
	57	GND	U	CPU	Power Supply return
	58	GND	U	CPU	Power supply return
	59	M1L	T	CPU	M1 Cycle
	60	A00H	T	CPU	Address Bus 00
25	61	A01H	T	CPU	Address Bus 01
	62	A02H	T	CPU	Address Bus 02
	63	A03H	T	CPU	Address Bus 03
	64	A04H	T	CPU	Address Bus 04
	65	A05H	T	CPU	Address Bus 05
30	66	A06H	T	CPU	Address Bus 06
	67	A07H	T	CPU	Address Bus 07
	68	A08H	T	CPU	Address Bus 08
	69	A09H	T	CPU	Address Bus 09
	70	A10H	T	CPU	Address Bus 10
35	71	A11H	T	CPU	Address Bus 11
	72	A12H	T	CPU	Address Bus 12
	73	A13H	T	CPU	Address Bus 13
	74	A14H	T	CPU	Address Bus 14
	75	A15H	T	CPU	Address Bus 15
40	76	A16H	T	CPU	Address Bus 16
	77	A17H	T	CPU	Address Bus 17
	78	A18H	T	CPU	Address Bus 18
	79	A19H	T	CPU	Address Bus 19
	80	PVCC	U	PS	+5 for personality
45					PROMs (VCC)
	81	GND	U	PS	Power supply return

82	GND	U	PS	Power supply return
83	PDB0H	U	All	Personality PROM Data bus 0
84	PDB1H	U	All	Personality PROM Data bus 1
85	PDB2H	U	All	Personality PROM Data bus 2
86	PDB3H	U	All	Personality PROM Data bus 2
87	PDB4H	U	All	Personality PROM Data bus 4
88	PDB5H	U	All	Personality PROM Data bus 5
89	PDB6H	U	All	Personality PROM Data bus 6
90	PDB7H	U	All	Personality PROM Data bus 7
91	PERSPROGL	T	Test	Disable Addr. & Data Busses
92	WAITL	U	All	MPU Wait input
93	+12	U	PS	
94	+12	U	PS	
95	-12	U	PS	
96	-12	U	PS	
97	GND	U	PS	
98	CLOCKL	T	CRT	CPU Phi clock
99	VCC	U	PS	+5 volts
100	VCC	U	PS	+5 volts

*TERMINATION: U = Unterminated
T = Terminated at each end of backplace with 330/390 ohm.

Referring now to Figures 11 and 11a, the CPU board is outlined in block format. Along with the standard Z-80A support hardware the main function of this board is to provide the address translation to obtain 1M byte of physical address space. By allowing the upper 7 bits of the Z-80 100 to address the mapping ram (plus 1 bit from an I/O register) up to 2, I/O selectable, maps are provided. These maps have a 512 byte granularity and would be set up during

program initialization. Logical addresses within the 1st four K defeat the address translation logic 102, so that the Eprom boot 106 and mapping ram can be accessed.

The CPU board contains 2 DMA control chips 108a and 108b. These are configured to allow memory-to-memory transfers, data transfers between the PCU and AMU and printer-plotter interfacing with 2 channels reserved for future expansion. Note: Only DMA channels 1 (DMA from AMU), and 7 (reserved degate the data bus driver between the backplane data bus and the internal Z-80 data bus. Therefore these are the only channels which can be used for DMA transfer to memory from a source on the system data bus. Note: Logic has been added to assert DMA2EOP when interrupt or NMI is asserted. This forces DMA on chip 2 to end (presently only memory to memory) when either interrupt occurs. As a consequence of this however the EOP interrupt from DMA chip 2 should never be armed. The printer interface employs a 64-character FIFO buffer 110 for data and a Z-80 PIO chip 112 for control. The printer-plotter will obtain its data via DMA, all formatting will be done under software control. The printer interface consists of an 8 bit port with handshaking, and several control lines, more fully explained hereafter. The port will present data to printer on a column by column basis, driving each printing wire independently, explained in more detail hereafter. There are two I/O selectable horizontal densities available; 4X, which places dots on 2.7 mil centers (2560 dots across 7"), and 1X; which gives 10.8 mil centers (640 dots across 7").

This allows less CPU and DMA overhead when printing alpha-numerics, as they require less resolution than high quality graphics. The keyboard is interfaced to the system via a PIO chip contained on the CPU board, explained in more detail hereafter.

The system is configured for various system options and line frequencies by setting jumpers to the following.

	Low (jumper in-place)	High (Jumper out)
Bit 0	60 HZ	50 HZ
Bit 1		
Bit 2		
Bit 3		
Bit 4		
Bit 5		
Bit 6		
Bit 7	(Jumper for odd Parity)	

Referring now to Figures 12 and 12a the display memory board contains the master oscillator and oscillator count down logic 120, the graphic memory 88 with associated multiplexers and registers, the grid memory 90 with associated multiplexers, registers, and translate proms and the video output driver 94.

The master oscillator 120 runs at 42.0MHz which is the output dot rate for the graphic and grid displays. The oscillator output is divided in half to make CLKH and again to make two phases of a quarter speed clock called CLKQA and CLKQB respectively. It should be noted that the full speed oscillator output does not leave the DISPLAY MEMORY board and the only other board receiving CLKH and CLKQ is the CRT CONTROL board.

The graphic memory 88 includes a 16K x 32 bit dual ported memory 88a, with one port driving the CRT and the other port available for CPU access. The dual port feature is achieved by time interleaving CRT and CPU accesses. The CRT accesses automatically perform the necessary dynamic memory refresh. This memory cycles at a rate of one cycle every 380.77ns resulting in a CRT fetch every 861.54ns. The output is loaded into a pair of 16 bit shift registers 88a and 88c (even bits and odd bits) which are clocked on opposite phases of CLKH and then multiplexed together to form the video output stream. The output also feeds a holding register 88c through a set of four to one multiplexers 88d organized such that this memory appears to the CPU to be a 64K x 8 bit memory. Provision is made to provide a clear function to this memory which functions during the CRT refresh cycles writing 32 bits at a time.

The clear function runs using the display scan and line counters to generate addresses. Note that the two high order bits of the line count indirect through the CRT Control Ram to select both the block address and the control function. Each CRT cycle will zero four bytes of memory by enabling all four write enables to the memory while forcing the input data to zero.

The grid memory includes a 1K x 8 bit dual ported memory 90a using bipolar memory which cycles in 95.19ns resulting in a grid fetch every 190.39ns. The output of this memory loads two holding registers 90b and 90c, one for CPU access and the other feeds the translate Proms 90d which feed a pair of 4 bit shift registers 90e and 90f clocked on opposite phases of

CLKH which are multiplexed to form the video output.

The translate process is performed using two proms each translating 4 bits of data under control of bits 6 and 7 of the control register located on the CRT control card, and two output bits from the line recode prom. The line recode prom examines the 6 low order bits of the line count provided by the CRT control card and develops a control sequence where:

0 blank (lines 61, 62, 63)
1 not a 6th line
2 a 6th line (0,6,12,18,24,30,36,42, 48,54,60)
3 reserved

The translate process consists of examining each pair of output bits (odd bit, even bit) and if both are set and this is not a sixth line converting both to zero, if this is a sixth line the 11 case translates to 01. Lines 61, 62, and 63 of each quadrant are blanked.

INPUT Odd	Even	6th Line	OUTPUT Odd	Even
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	0	0
0	0	1	0	0
0	1	1	0	1
1	0	1	1	0
1	1	1	0	1

The Grid Memory 90 cycles continuously for both CRT refresh and CPU access. The CPU access reads data present at the address selected by the low 10 bits of the address regardless of the upper address

bits, however the data is only gated to the bus if the high address together with MEMRQ and READ selects the grid memory. Since the Address Bus (especially the nontranslated address) is valid long before MEMRQ it is possible for the data to be present in the output register before MEMRQ is asserted.

The video driver circuit 94 sums the signals from the graphic output, the grid output, the alphanumeric output and the cursor output from the CRTC to form the video drive to the display.

Referring now to Figures 13 and 13a, the CRT CONTROL board contains the alphanumeric memory 92, the alphanumeric character generator 92a and shift register 92b, the CRTC chip 122, the address decode 124 and wait state generation 126 for both the CRT control 128 and the display memory, the CRT control registers 130, the PROM sequencer 132 for generating memory timing and the CPU clock, the PROM sequencer 136 for generating CRTC timing, and the line and scan counters 132 and 134.

The alphanumeric memory 92 includes an 16K x 8 dual ported memory 138, with one port driving the CRT and the other available for CPU access. The memory cycles at a 333.17ns rate resulting in a CRT fetch every 666.35ns. Each alphanumeric dot is 4 graphic dots long with 7 dot times per character. (Thus the CRT output register must be loaded every 28 periods of the master oscillator.) The memory output is staged into the character generator ROM 92a and on to the output shift register 92b. The output of this shift register 92b is "ex-ored" with the twice delayed bit 7 from the memory to provide the reverse video feature. The CRT cycles are addressed from the CRTC chip 122 which also causes the dynamic memory to be refreshed.

The CRTC chip 122 is a Motorola MC6845 CRT controller or any other compatable controller which provides alphanumeric memory addressing, vertical and horizontal sync, row addresses for the character generator, alphanumeric display enable and cursor video. The timing signal ANADRMXBL which swings the address multiplexer between the CRT and CPU addresses is used to generate the character clock to the CRTC 122. The CRTC register 0 may be accessed at I/O address 48 and register 1 at address 49. (Addresses 4A-4F also map into these registers.)

This card supplies CPU address decoding for the DISPLAY MEMORY card, and provides wait signals for both the graphic and alphanumeric memories as well as the CRTC. The wait for the alphanumeric and graphic memories is generated by the main timing PROM sequencer 132 and is optimized for minimum CPU cycle times.

The CRT control registers 130 are dual ported registers at I/O addresses 40-43 corresponding to the four quadrants of the screen. (Each quadrant is 64 lines of the display screen and are numbered sequentially from the top starting with zero.) In addition locations 44-47 are decoded as addressing other registers in this bank and may be loaded and read but perform no control functions.

Bits 1 and 0 select the bank (16K) of graphic memory to be displayed in this quadrant.

Bits 3 and 2 control the graphic display:

BIT 3	BIT 2	FUNCTION
0	0	display
0	1	blank
1	0	reserved for future use
1	1	clear bank of memory

Bits 5 and 4 select the bank (256 words) of grid memory to be displayed in this quadrant.

Bits 7 and 6 control the grid display:

BIT 7	BIT 6	FUNCTION
0	0	blank
0	1	display without translatior
1	0	display with translation
1	1	reserved for future use

The main PROM sequencer 132 generates the timing controls for the alphanumeric memory 92, the graphic memory 88 and the CPU clock as well as providing the wait state control 126 for accessing these memories. The sequencer 132 cycles at a 95.19ns rate and provides a timing resolution of 47.6ns for some signals by loading 2 bits to 2 bit shift registers which run at this rate. The sequencer 132 provides alphanumeric cycle timing which repeats every 7 words, graphic memory timing which repeats every 8 words and CPU timing which repeats every 3 words. Thus 7 x 8 x 3 = 168 words of storage are required to provide an integer number of each pattern. This provides every possible phase of these signals. It should be noted that one horizontal line consists of 92 character times which is equivalent to 80.5 graphic load cycles, 322 grid loads, 214 2/3 CPU clocks and 15 1/3 sequence cycles. The CPU clock should free run but the graphic timing should be even for each line on the display. To accomplish this it

is necessary to jump over 84 locations in the sequence. This is accomplished by storing the 168 words as two banks of 84 words on 128 word boundries and inverting the high order address bit of the sequence memory one extra time per line. This results in two CPU access cycles occurring in a row once per line during horizontal retrace. To insure that these two cycles occur at the correct phase of the graphic cycle during horizontal retrace the CRTC 122 (which generates horizontal and vertical sync timing) is phased to the main PROM sequencer 132 using a CRTC clock swallowing technique until the horizontal sync occurs at the correct phase of the sequencer. Logic is also provided to inhibit the generation of two CPU cycles in a row if the CRTC is not yet correctly phased. This protects the memory from getting narrow strobes. The grid timing consists merely of establishing the phase of the CPU and CRT cycles and is based on the low order bit of the sequence address counter. The alphanumeric and graphic wait state controls 136 are based on forcing wait states until a correct phase of the appropriate memory and then both starting the access and switching to determining the wait states based on sequence memory outputs (with patterns which repeat every 21 and 24 words respectively).

The CRTC chip 122 requires a free running clock 142 to the ENABLE input at a rate between 100KHz and 1MHz this signal together with the chip select and a signal to end the wait state are provided by a second PROM state sequencer 140 using a 32 word PROM 144 and a recirculating register 146. It should be noted that the high order address to the PROM 144 is a latched version of ADRCRTCL which indicates that the

CPU is accessing the CRTC. The sequencer 140 cycles between addresses 10-13 generating ENABLE until ADRCRTCL is asserted at which time it jumps to what would have been the next address except with address bit 4 reset (00-03). From here the routine jumps into the process routine in such a way that the ENABLE cycles are not disturbed and proper setup is provided for the process cycle. The process routine asserts CS to the CRTC and at the proper time asserts a control to set the CYIP (cycle in progress) flip flop which causes the CPU wait line which was held asserted to be deasserted. The sequencer then waits for the CPU to deassert the signals making ADRCRTCL in a loop (OD-OF .04). When the CPU causes ABRCRTCL to be deasserted the high order address bit comes on which causes the sequencer to jump into a state which vectors the sequence back to the inactive loop (10-13).

The line and scan counters 132 and 134 provide addressing for the graphic and grid memories 88 and 90. The scan counter 134 is an 8 bit counter (256 states) incrementing every 190.39ns. thus this count increments once for each grid load and by four for each graphic load. The counter 134 is preset on each horizontal retrace such that the graphic memory 88 starts each line at scan count zero. Since only one counter is provided and the grid features an extra stage of delay the grid displays location FF followed by location zero. The line counter 132 is incremented once per horizontal line during retrace and is preset during vertical retrace such that the top displayed line on the screen corresponds to a count of zero.

Referring to Figure 14, the EPROM board 150 is straight forward, with full address (20 bits) decoding required. One wait state will be required on all memory accesses. A 64K x 8 array will be supported using 2716 16K EPROMS. The board is designed such that all EPROM's are programmable from the card edge. Address strapping is required to assign a block of 64K of physical address space to these boards.

Referring now to Figures 15 and 15a, the I/O board contains a multi-pupose timer chip 160, a dual-port modem interface such as a Zilog DART or any other compatable component, a system resent generator 162, the interface 164 to the non volatile memory board 66, and the docking interface logic 168 for the AMU. The I/O board also contains an 8-channel analog to digital converter 168 which allows the software to measure system power supply voltages, logic and memory voltages in the AMU, and the battery condition in the AMU so that an estimate may be made of remaining battery life. An 8-bit D to A converter 170 is also included to generate diagnostic test signals for the AMU.

The DART 160 interfaces two RS-232 compatible asynchronous modem interface channels supporting: Ring Indicator, Data Terminal Ready, Request to Send, Clear to Send (without additional delay provisions), Data Carrier Detect, Transmit Data, and Receive Data. Provision is made to sense Data Set Ready externally to the DART 160.

The reset generator 162 allows the program to generate a system reset for 500 Msec. or until Non Maskable Interrupt is deasserted.

The real time clock 172 on the non volatile memory board is an OKI MSM5832 which is interfaced by a PIO 112 for its data bus, the low four bits of the DAC data holding register 174 for address, and an addressable latch 176 for the other control signals (except CE which is provided on the NVM board from a power ok detect circuit). The interface to the non volatile memory 166 is straightforward except that bit 7 of addressable latch 0 (I/O Adr: 50) must be set to allow this memory to be written.

The AMU interface consists of logic 180 to decode AMU addresses, DMA input and output circuits 178a and 178b, a PIO trapping data read by the AMU processor from its A/D converter 168, and addressable latches 176 supplying various control signals.

Referring now to Figure 16, the non volatile memory board is a daughter board attached to the back of the I/O board. This board contains up to 16K of memory 166 and a real time clock chip 12 which are provided with NICAD battery 182 backup. The bulk of the interface logic to this board is present on the previously described I/O board. Charging current to the battery is provided from the system +12V when the PCU is powered up and also from a separate transformer 184 which is only energized when the PCU is powered down. This board is designed to maintain data and time when detached from the system. Provision is made on this board to allow the installation of a second battery if reliability problems arise with a single battery version.

Referring now to Figure 17, the AMU Interface consists of two boards: the Digital board is attached to the back of the docking station and the analog board is mounted to one side of the CRT.

The AMU interface board contains interface drivers and receivers 186 for the AMU, the dock/undock solenoid 188 with drivers 188a and the buzzer 190. The AMU interface drivers and receivers 186 are CMOS and are powered through diodes from both the PCU and the AMU (V1). The chip select for these components is generated from a circuit 190 which monitors power such that the chip select will only be true if both PCU +5 and AMU V1 are up and PCU SYSRESL is false.

The solenoid 188 is controlled such that it is energized through a dropping resistor when the AMU is partially inserted but not yet seated in the connector or it may be fully energized under software control.

The front panel Patient connector 22 is cabled to this card which contains the isolation amplifier(s) to isolate and buffer the patient leads. These amplifiers feed an analog mux 192 which allows test signals (from the DAC on the I/O Board) to be substituted for the live signal either as lead 1, lead 2 or both (common mode rejection test). Provision is made to support the "four lead" patient connection with a second isolation amplifier and amplifier synchronizing drive.

The keyboard assembly shall contain encoding electronics such that a uniquely encoded 7 bit data word and strobe are available at the output port. The keyboard will be of the "upstroke-downstroke" type, i.e. a strobe is generated twice

for each key stroke. This allows great flexibility for the software in encoding specialized function keys. There are 54 alpha-numeric and defined control keys, and 20 undefined "function" keys. However, all keys are defined in software, therefore this is alterable by simply changing keytops. Note also that the keypad layout can be changed later, as further definitions of the keypad functions are developed. The bezel covering the keyboard will be replaceable to accommodate these changes.

This CRT Video Drive Board and Display uses a raster scan display driver with video, horizontal sync and vertical sync each as a separate signal.

The CRT video board and CRT are a purchased assembly. The board contains the high-voltage supply, horizontal and vertical sync, and video modulation circuitry. The interface definition is set forth more fully hereafter.

Where possible, all user-control functions will be initiated via the keyboard, (i.e. the software will control the definition and execution of most functions). This approach maximizes the flexibility of the system. The following exceptions exist:

The power-on switch will be located on the back panel of the CRT housing.

The brightness control is on the outside right edge of the PCU, and interfaces directly to the CRT video board.

A momentary push button which is pushed concurrently with (overlapping) the resent control will cause a reset to the diagnostic operating system.

The following section gives I/O port definitions and system programming details:

For software purposes the screen can be considered as 3 overlapping display pages which are logically "or'ed" to produce a visual display.

The Graphic Memory contains four blocks of binary image of the screen, each 64 rows long by 2048 bits (256 bytes) wide. Each block may be assigned to one or more quadrants of the screen under control of the CRT Control registers, as shown below:

QUADRANT 0

QUADRANT 1

QUADRANT 2

QUADRANT 3

CRT Quadrant Assignment

The Grid Memory also contains four blocks, each 2048 bits wide however only one row is stored for each block of 64 lines. The data may be passed through a translate structure which allows forming a grid image. The translate process consists of examining each pair of output bits (odd bit, even bit) and if both are set and this is not a sixth line converting both to zero, if this is a sixth line (0,6,12,18,24,30,36,42,48,54 or 60) the 11 case translates to 01. Lines 61, 62 and 63 of each quadrant are blanked.

The CRT control registers are dual ported registers at I/O addresses 40-43 corresponding to the four quadrants of the screen. In addition locations 44-47 are decoded as addressing other registers in this bank and may be loaded and read but perform no control functions.

The clear function runs using the display scan and line counters to generate addresses. Thus this function will take an arbitrary amount of time to complete as a function of the phasing between the setting of the clear command and the count in these counters. One method of determining that the clear is complete is to start the clear and then write a nonzero byte to the lowest location in the quadrant and the highest location in the quadrant. If these bytes are zero on the next 60Hz interrupt then the clear is complete. Waiting two 60Hz periods also will guarantee that the clear is complete. Note that if only one block is to be cleared and more than one quadrant is blanked to the screen that multiple CRT Control registers may be used to clear the block which will speedup the clear.

The alpha-numeric control is centered around an LSI CRT control chip, such as the MC6845 or any compatable component. The chip controls the display of ASCII characters stored in a 16K byte buffer. There are nineteen registers in the CRTC chip which are accessable to the CPU. All I/O to 18 of the registers is done indriectly, via the pointer stored in the 19th register. (address register-I/O Address 48). During initialization the CRTC must be programmed to support the particular monitor in use. Note that all I/O is executed to one of two ports, the address register (48) or a data register (49).

Note: The first character position on the screen corresponds to a cursor position of 1 and there is an extra cursor position at the start of each additional line.

Note: The above listed value for R1 is for 72 characters per line. For 73 characters per line load R1 with "4A".

The alphanumeric data is translated into a series of dots to be displayed by a character generator ROM according to the patterns shown in Figure 19. Reverse video (dark characters against a lighted background) will be generated if the high order bit of the displayed byte equals 1.

The data to the printer is to be output in 8 bit bytes via DMA transfer. There will be two horizontal dot resolutions which are software selectable, 1X - (.0027 inch) and 4X - (.0108 inch). This gives 2560 dot positions across an 6.912 inch page (in 1X mode) or 640 positions in 4X mode. The 4X mode is intended to save memory space and microcomputer overhead when alphanumerics are being printed. The data should be formatted in n x 2560 byte blocks, such that the dma transfer can be re-initialized during the carriage return or "dead time" of the printer head. Using the rotary printer in 1X mode, results in a data transfer rate of about 120K bytes/sec (8.295 micro-seconds per point). This is only required during the action portion of the print head cycle, which in the case of the rotary printer is 1/3 of the overall printing time. Note that the system software is responsible for formatting all data into bit patterns capable of driving the print head on a one to one basis.

The start-stop timing of the printer is controlled by software to allow consistent stop distances. The start distance is controlled by counting REV interrupts. A "worst case" standard number of revolutions will be allowed (3?), so that standard spacing can be maintained. The stop distance will be determined during the power-up initialization routine by the following procedure. The printon bit is set and after the standard number of revs a short test message can be printed. Immediately before stopping the printer (by resetting printon) the CPU CTC counter channels 2 and 3 are initialized to count dotsense transitions. After a predetermined period of time it can be assumed that the printer has stopped and the count can be read. The count will represent the distance the printer stopped in, this count can then be used to determine when to reset the printon bit to achieve a constant stopping distance. For example; assume a count of 12,000 was read after the test stop, and it was determined that "worst case" a stopping distance of 18,000 could be achieved by any printer. Then the CTC would be setup to interrupt after 600 dotsense transitions were received, and the printon bit reset. Thus a total stopping distance of 18,000 could be maintained. The last stop distance can be used to determine the next brake point, thus it becomes an iterative process which will track the dynamics of the printer.

The Keyboard is an upstroke/downstroke type wherein a strobe and a dataword is generated both on the pressing of a key and the release. This data is interfaced through port A of the PIO at

address 08-OB and the controls through port B. Operation of the keyboard is as follows: When a key is depressed on keyboard asserts the data corresponding to this key on the data lines (bits 0-6. data bit 7=low) and then asserts strobe. The program in the PCU should recognize this strobe, sample the data and then assert keyboard acknowledge. The keyboard will then deassert its strobe at which time the program should deassert acknowledge. Note: The acknowledge signal should be deasserted within 10 microseconds of the deassertion of strobe. When a key is released the same process is repeated except that data bit 7 is high. The repeat function is supported by the program causing repeat to be asserted at least 1 microsecond prior to acknowledge of the character to be repeated. This will cause the keyboard to generate multiple strobes. Any action on the keyboard (upstroke or downstroke) will cause the keyboard to cease repeating and present the new code. See Figures 20 and 21 for Keyboard code assignments and Keyboard key assignments.

There are two asynchronous communication ports provided, which are RS-232 compatible and lead to external connectors. The baud rate of each channel of the DART is set up by programming (see section 6.3) the timer chip (at I/O port 3C-3F section 0 for channel A and section 1 for channel B) to provide the proper buad rates. For detailed initialization info and programming examples see the manufacturer's product specification (Z-80 DART which also references the

Z-80 SIO specification), Note that only control register WRO is directly accessable, it contains a pointer to the other write registers. The read registers are accessed in the same manner. Note also that all registers are duplicated for both channels (except RR2, channel B only).

The Analog to Digital converter is provided to monitor both the PCU and docked AMU power. This ADC is a National ADC0809 and contains an internal 8 input analog multiplexer which is controlled by writing an internal register.

The ADC is operated by writing the I/O port 53 the data given (this selects the input channel) and then issuing start (write "60" to I/O port 53). The end of convert (EOC) signal (DBO) at read I/O port 51) will go false within 10 microseconds and will go true again when data is valid in the output register (read I/O port 50). The ADC requires less than 85 microseconds to perform a conversion.

The VB1 and VB2 lines (AMU batteries) may be checked with additional load by asserting Enable Test Load (on: "OE", off: "06" to I/O address 50). Note: This test draws significant current from the batteries and therefore the Enable Test Load signal should be asserted for the shortest practicable time (VB will off load the AMU current from the batteries but not the test load).

The PCU is capable of supplying external power to the AMU and controlling the AMU power supplies. Each of these functions is program controlled.

Supply VB provides external power to the input of the voltage regulators and effectively off loads the batteries. This feed is switched on by writing

"OD" to I/O address 51 and switched off by writing "05".

Supply VM is asserted by writing "OF" to I/O address 51 and turned off by writing "07". This line supplies VM and causes the VM regulator in the AMU to start, thus VM will remain on when this supply is deasserted.

Supply +5V AUX (on: "OE", off: "06" to I/O address 51) powers the personality/bootstrap PROM and causes the VL regulator to start. Note: The AMU processor has a command which will turn off VL.

Clamp VR (on: "08", off: "00" to I/O address 54) pulls down the reference voltage to the AMU regulators and will cause them to turn off. WARNING: Shutting down VM will cause the AMU memory to lose data.

AMU I/F Ena must be asserted to allow operation of the interface but should be deasserted prior to powering down VM (VRel clamp).

AMU Reset, Docked and Prom Ena ena are controlled only by the PCU software while Interrupt is also deasserted by the AMU reading its I/O address 07.

Input ready and Output ready are discussed in more detail below.

PROM ENA to the AMU is generated by ending Prom Ena ena with AMU read and the decode of the low 32 bytes of AMU address qualified with AMU IO/M.

The AMU may read status consisting of Input ready (on bit 1) and Output ready (on bit 2) by reading I/O address 04.

Data transfer to the AMU is by DMA on the PCU side and programmed I/O on the AMU side. DMA channel A feeds an output register which is read by the AMU at AMU I/O address 07. Reading address 07 also clears Interrupt

and Input ready. Input ready is asserted by the DMA channel when it loads the output register. Input ready being deasserted causes DMA request to channel A and thus Input ready will cycle for each byte transferred.

Data transfer from the AMU is DMA on the PCU side using DMA channel B and programmed I/O on the AMU side writing I/O address 07. Output ready may be cleared by the AMU writing to I/O address 06 and this is the normal end of a data transfer. Output ready will remain asserted for the entire duration of the DMA read.

Whenever the docked AMU reads data from its ADC by reading I/O address 01, the data is also loaded into the PCU PIO at address 34-37 channel B using PIO strobe B.

An 8 bit Digital to Analog Converter is provided which is capable of driving lead 1, 2 or both of the AMU. The DAC follows the contents of the DAC holding register which is written at I/O address 52. All zeroes to the DAC corresponds to 3.75V out while "FF" corresponds to 1.25V. The DAC settles in less than 100 ns. Note: The DAC holding register (4 lsb) also act as the address holding register for the real time clock.

Lead control is provided by 2 bits from addressable latch 0 (I/O write address 50). To drive lead 1 only write 02 and 03 to I/O address 50. Lead 2 (inverted data) is selected by writing 09 followed by 03. Both leads (common mode rejection test) is selected by writing 02 followed by 0A. Patient leads are attached by writing 09 followed by 0A. Power up places the system in the lead 1 state.

Writing 0D to I/O address 50 should cause the AMU to be ejected from the PCU by activating the solenoid. AMU Present will be deasserted when the AMU is successfully undocked and the solenoid should be deactivated 250-500 ms. later. A software time out of 5 sec. should be provided on activation of the eject solenoid.

The real time clock chip used is the OKI MSM5832 which contains a crystal oscillator, clock/calendar counters and interface although any other compatable component well known in the art could be used. This device is interfaced using bits 0-3 of PIO (at I/O address 34-37) port A for the data bus, the low 4 bits of the DAC holding register (I/O address 52) supply the address and the control lines are supplied from addressable latches.

The buzzer is a piezoelectric device driven from CTC (I/O address 3C-3F) channel 2 through an additional divide by two if enabled by writing "0C" to I/O address 50 (inhibit by writing "04"). This device is expected to be most efficient when operated at frequencies around 2.5 KHz.

The LSI timer chip used is the Z-80A/CTC IC. It includes 4 separate channel timers, along with appropriate interrupt logic such that interrupts can be generated on a variety of events. The Zilog technical manual details the programming techniques and modes available, while section 6.10 outlines the I/O port assignments and bit mnemonics.

The CTC chip at I/O address 04-07 is hardware

configured as 2 cascaded timer groups. Channel 0 is programmed in the timer mode and thus receives the system 3.503 Mhz clock as the timing input. Channel 1 is programmed in the counter mode and receives the output pulse from channel 0 as the timing input. In this manner, software may program timing interrupts as desired over a broad range. Channel 2 is programmed in the counter mode and receives the output pulses from channel 2. In this manner, the software can determine the dynamic characteristics of the printer so that braking signals may be properly generated.

The CTC chip at I/O address 3C-3F channels 0 and 1 supply the DART clocks for channel A and B respectively and are driven from a 307.16 KHz source. Channel 2 feeds an additional divide by 2 which feeds the buzzer (Note: The buzzer has a separate enable so this timer may be used for other purposes). Channel 3 clock input is cascaded from channel 2.

Seven channels of Direct Memory Access Control (DMA) are provided using 2 AMD 9517A (Or Intel 8237-2) ICs. Channel 0 of DMA chip 1 (I/O address 10-1F) supports DMA to the AMU, channel 1 supports DMA from the AMU, channel 2 supports DMA to the printer and channel 3 is used to cascade to the second DMA controller chip (control and priority resolution: this channel does not move data). Channel 0 of DMA chip 2 (I/O address 20-2F) is the source control for DMA memory to memory move, channel 1 supports the destination control for memory to memory while channels 2 (DMAREQC/DMAACKS) and 3 (DMAREQD/DMAACKD) are reserved for future expansion.

Note: DMAEOP to chip 2 is asserted by the printer buffer needing data or either interrupt or non maskable interrupt. Thus the DMA controller will break out of DMA whenever the printer needs data or an interrupt occurs. This also means that if interrupt is enabled for chip 2 an interrupt will be generated for each printer data burst and for each other interrupt a second interrupt will occur.

By translating the upper 7 bits from the Z-80 to 11 bits, via a 256 x 12 ram, a 1M physical address space is provided. This allows 2, I/O selectable, "maps" with a 512 byte granularity. Since the translation ram must be able to be written to and read from, it must occupy a section of Logical Memory where no translation is allowed. This is also true of the 2K EPROM boot and of the Grid and Caliper memory (because of speed requirements). The lower 4K is reserved for these functions, i.e. the physical and logical addresses are the same. The translation RAM is organized as two blocks of memory for program read/write. The lower block forms the lowest 8 bits of the translation (which becomes address bits A09-A16), while the lower 3 bits of the upper block become the higher order bits (A17-A19). The 4th bit (bit 3) of the upper block if reset inhibits write to this page of memory. The upper four bits of the upper block are not backed by memory devices and data written there will be don't care while data read will be undefined.

The non translated memory space is not write protected. Translated memory space is protected to the page level by bit 3 of the upper block of translate ram which if reset (0) will inhibit write to that page.

The non volatile memory has an additional protection flip flop which protects this entire memory. Writing is enabled by writing "OF" to I/O address 50 and inhibited state.

The Boot EPROM and main EPROM memories have one wait state per access.

The Translate RAM and Non Volatile memories operate without wait states.

The Grid memory operates without wait states however the translation process adds sufficient delay that this memory may no longer fetch instructions correctly. The grid memory may be read, written or executed when accessed with a non translated address but may only be read or written when accessed through a translated address. That is, the Grid memory should not be used to execute programs in virtual space.

Since both the graphic and alphanumeric memory timing is sliding in phase with respect to the CPU clock the number of wait states will vary from operation to operation.

The hardware interrupt mechanism will consist of a 16 level daisy-chain structure with hard-wire priority levels. The Z-80A "mode 2" interrupt response is supported, as all interrupting devices will respond with a 8 bit address vector when so requested. The Z-80A interrupt response is covered in detail in the CPU technical manual. The Z-80 system interrupt protocol for nested interrupts will be maintained, i.e. higher priority devices may not interrupt a lower priority device until its interrupt service routine is completed.

The timing constraints on the interrupt daisy chain are resolved by using a "look-ahead" configuration of 74LS08 gates to rapidly propagate the "disable"

condition to the last element in the chain. The slow operation of the "enable" condition, which occurs during RETI with a pending high-level interrupt, is compensated by inserting a number of WAIT states between the 2 bytes of the RETI instruction. Hardware assumes that an EI instruction is always present immediately before the RETI; therefore, this instruction is decoded and used to trip the wait state generator. Failure to include an EI immediately before the RETI causes an exposure to lost RETI operation at the end of the daisy chain.

Provision is made on each card for up to 4 interrupting devices, and the daisy chain connections for each one are brought out to the backplane so that priority may be assigned as necessary.

Each pluggable card in the system shall contain a personality PROM. The PROMs are accessed via indexed I/O instructions; therefore, the addressing of the PROM is derived from the upper 8 bits of the system address buss, and the chip select is derived from the I/O port address. The outputs of the PROMs are connected to a separate PROM data buss on the backplane to facilitate PROM configuration and alteration on assembled cards. The PROM data buss is routed to the system data buss when the PROMs are accessed by the appropriate I/O instructions.

Due to the separate data buss employed for the personality PROMs, the chip select requires only the low 4 bits of the address buss. The remainder of the necessary gating is done on the CPU board by the buss transfer gates during the input instruction.

The PROM chosen for use is a 256 bit part organized as 32 words of 8 bits each.

Industrial Applicability

The ambulatory monitoring unit may be sold to or used by medical personnel or medical facilities for patient analysis or control to provide better medical care.

The instant invention has been shown and described herein in what is considered to be the most practical and preferred embodiment. It is recognized, however, that departures may be made therefrom within the scope of the invention and that obvious modifications will occur to a person skilled in the art.

Claims

1. A patient monitoring system for a patient having monitorable signals, comprising: an ambulatory container, a monitoring means connected to said container, said monitoring means for monitoring of ambulatory patient output signals, real-time analysis of said signals and storage of analyzed signals for indepth reporting of said monitored and analyzed ambulatory patient output signals, said monitoring means includes power means for supplying power to said monitoring means, acquisition and conditioning means for acquiring and conditioning the ambulatory patient output signals to provide conditioned output signals, said acquisition and conditioning means connected to said power means and connectable to the ambulatory patient, detection and management means for detecting and managing the conditioned output signals for identification, said detection and management means connected to said acquisition and conditioning means, identification means for identifying particular conditioned output signals, said identification means connected to said detection and management means, pattern classification means for classifying particular patterns and change in the particular conditioned output signals in real-time, said pattern classification means connected to said identification means, storage means for storing the classified patterns and changes, said storage means connected to said pattern classification means; and output means for providing output from storage means, said output means connected to said storage means.

2. A patient monitoring system for a patient having monitorable output signals comprising: a power supply; interface means for receiving and generating patient data, electrically coupled to said power supply; analyzing means for storing and analyzing said patient data, electrically coupled to said interface means; processor means for controlling the flow of said patient data, electrically coupled to said analyzing means; display means for displaying said patient data, electrically coupled to said processor means.

3. A patient monitoring system as set forth in Claims 1 and 2, wherein: said ambulatory container having docking means interconnectable to said interface means, said docking means electrically coupled to said storage means and said detection and management means; said display means providing immediate display of said patient data from said storage means for physician interpretation in patient management when said docking means is connected to said interface means; said interface means also for generating preselected patient data through said docking means into said detection and management means for comparison with patient output signals when said docking means is connected to said interface means.

4. An ambulatory patient monitoring method for an ambulatory patient having monitorable signals, for monitoring of ambulatory patient output signals, real-time analysis of said signals and storage of analyzed signals for indepth reporting of said monitored and analyzed ambulatory patient output signals by a monitoring device comprising the steps of: connecting the monitoring device to the ambulatory patient, supplying power to said monitoring device, then acquiring and conditioning the ambulatory patient output signals to provide conditioned output signals, then detecting and managing the conditioned output signals for identification, then identifying particular conditioned output signals, then classifying particular patterns and change in the particular conditioned output signals in real-time, then storing the classified patterns and changes; and for providing analyzed output from said storage upon call for such data.

5. An ambulatory cardiographic monitoring system, comprising: a data collection means including, a signal carrying means electrically responsive to a patient's heartbeat signals, an amplification means for amplifying said signal into converible form, said amplification means connected to said signal carrying means, a converting means for converting said analog heartbeat signals to digital signals, said converting means connected to said amplification means, a data processing means for processing input data for storage, said data process means electrically connected to said collection means, said data processing means including, programming means for providing a programmable read only memory and for providing manual priority changes in said data processing means, memory means for storage of preset template means and for storage of said processed data output signals, said memory means connected to said programming means for comparing said digital signals to said preset template means for generating a digital output for storage in said memory means, said processor means connected to said programming means and said memory means a readout connection means electrically connected to said digital output and connectable to a converting means for converting said digital output signals to display signals, and a power control means connected to said data collection means and said

data processing means, said power control means for supplying electrical energy to said monitoring system.

6. An ambulatory cardiographic monitoring system as set forth in Claim 5, wherein: said collection means includes a filter means for rejection of induced body noise connected to said amplification means.

7. An ambulatory cardiographic monitoring system as set forth in Claim 5, wherein: said control means includes, a battery means, a logic means for regulating the electrical energy to a standby level upon low energy level to preserve stored processed data.

8. An ambulatory cardiographic monitoring system as set forth in Claim 7 including: a readout means electrically connectable to said monitoring system, said read out means including converting means for converting said digital output signals to analog signals, and display means for providing a visual representation of said analog signals.

9. An ambulatory programmable digital patient monitoring system, comprising: an analog data collection means for receiving and converting analog electrical signals to digital form, said analog data collection means including an input and output; a programmable digital processing means for receiving programs, processing said electrical signals in digital form, in accordance with inputted programs to provide critical digitalized data and storing said critical digitalized data, said programmable digital processing means connected to said analog data collection means output, said programmable digital processing means including an input and output; a storage means for storing input data connected to said output of said processing means; a carrying means for carrying said analog data collection means and said programmable digital processing means, said carrying means including connecting means for connecting said analog data collection means to a patient to provide an ambulatory monitoring system; a portable power supply means connected to said analog data collection means and said programmable digital processing means, said portable power supply means for providing a power source; said analog data collection means, said programmable digital processing means and said carrying means for providing an ambulatory programmed digital patient monitoring system for analysis of patient

electrical signal output functions in real-time for storage in memory in a minimum number of bits of digital data to provide storage capacity in terms of days and real time monitoring.

10. An ambulatory programmable digital patient monitoring system as set forth in Claim 9 wherein: said processing means including a plurality of input template means for comparison with input data for processing for storage of heart data.

11. What is shown and described herein.

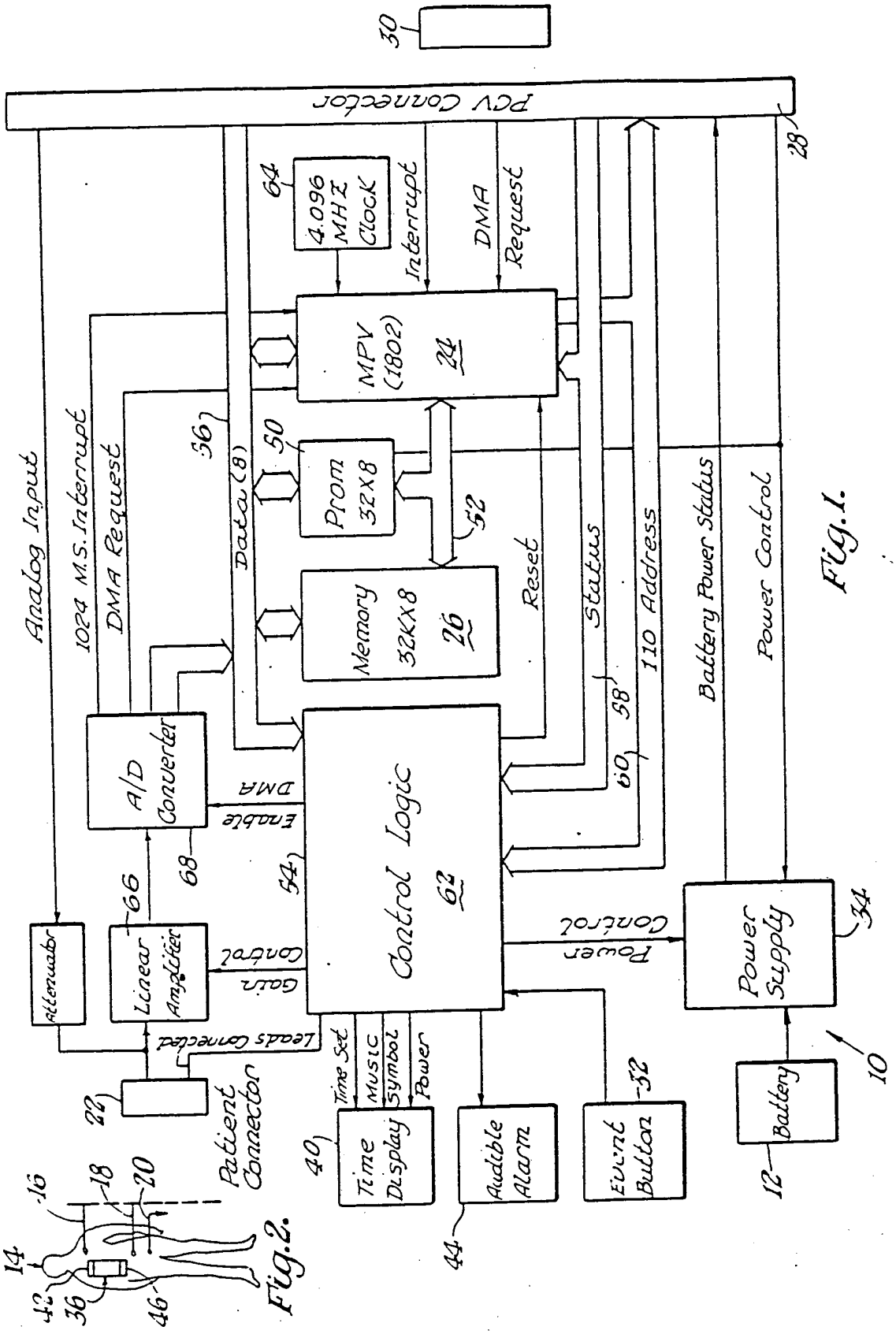

30
PCV Connector
28
64
4.096 MHZ Clock
Interrupt
DMA Request
MPV (1802)
24
Analog Input
1024 M.S. Interrupt
DMA Request
36
Data (8)
50
Prom 32X8
52
Memory 32KX8
26
Reset
Status
58
110 Address
Battery Power Status
Power Control
A/D Converter
Enable DMA
68
54
Control Logic
62
60
66
Attenuator
Linear Amplifier
Gain Control
Power Control
Power Supply
34
Leads Connected
22
Patient Connector
Time Set
Music
Symbol
Power
40
Time Display
Audible Alarm
44
Event Button
32
Battery
12
10
16
18
20
14
42
36
46

Fig. 1.

Fig. 2.

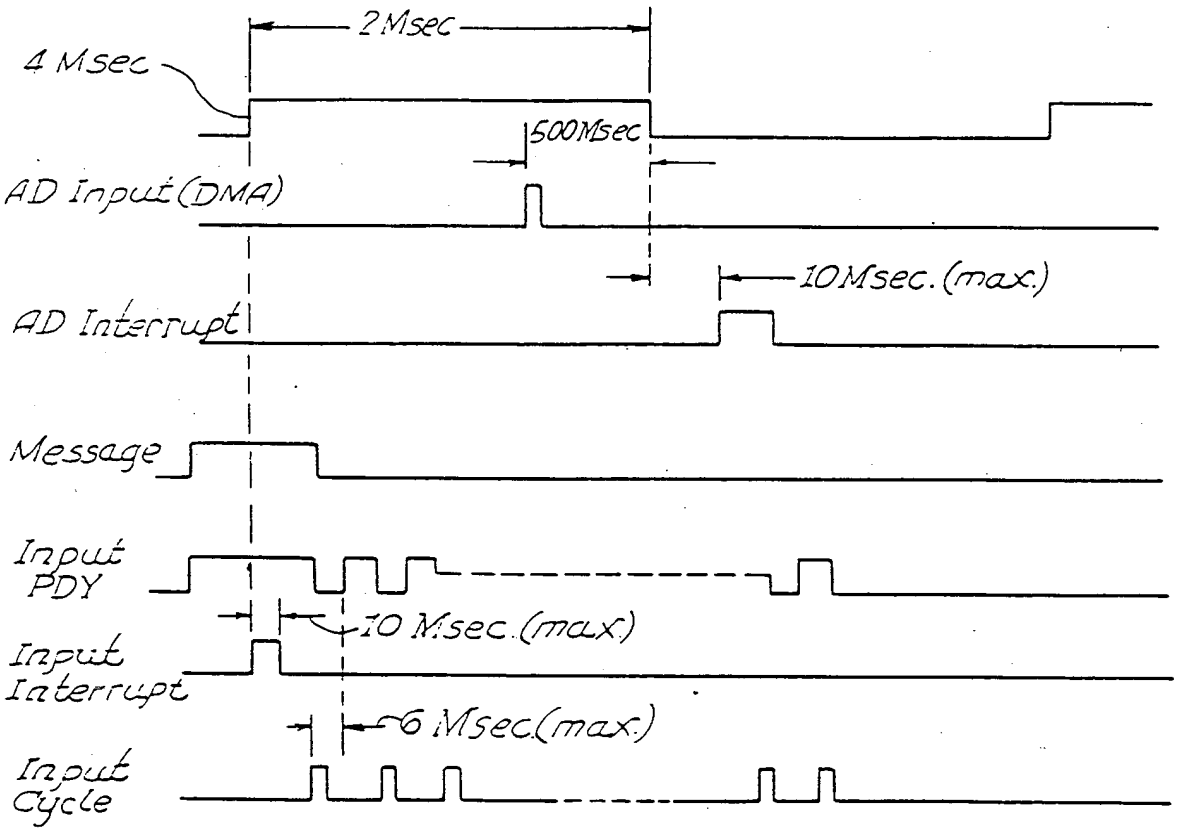

2 Msec
4 Msec
500 Msec
AD Input (DMA)
10 Msec. (max.)
AD Interrupt
Message
Input PDY
10 Msec. (max)
Input Interrupt
6 Msec. (max.)
Input Cycle

Fig. 3.

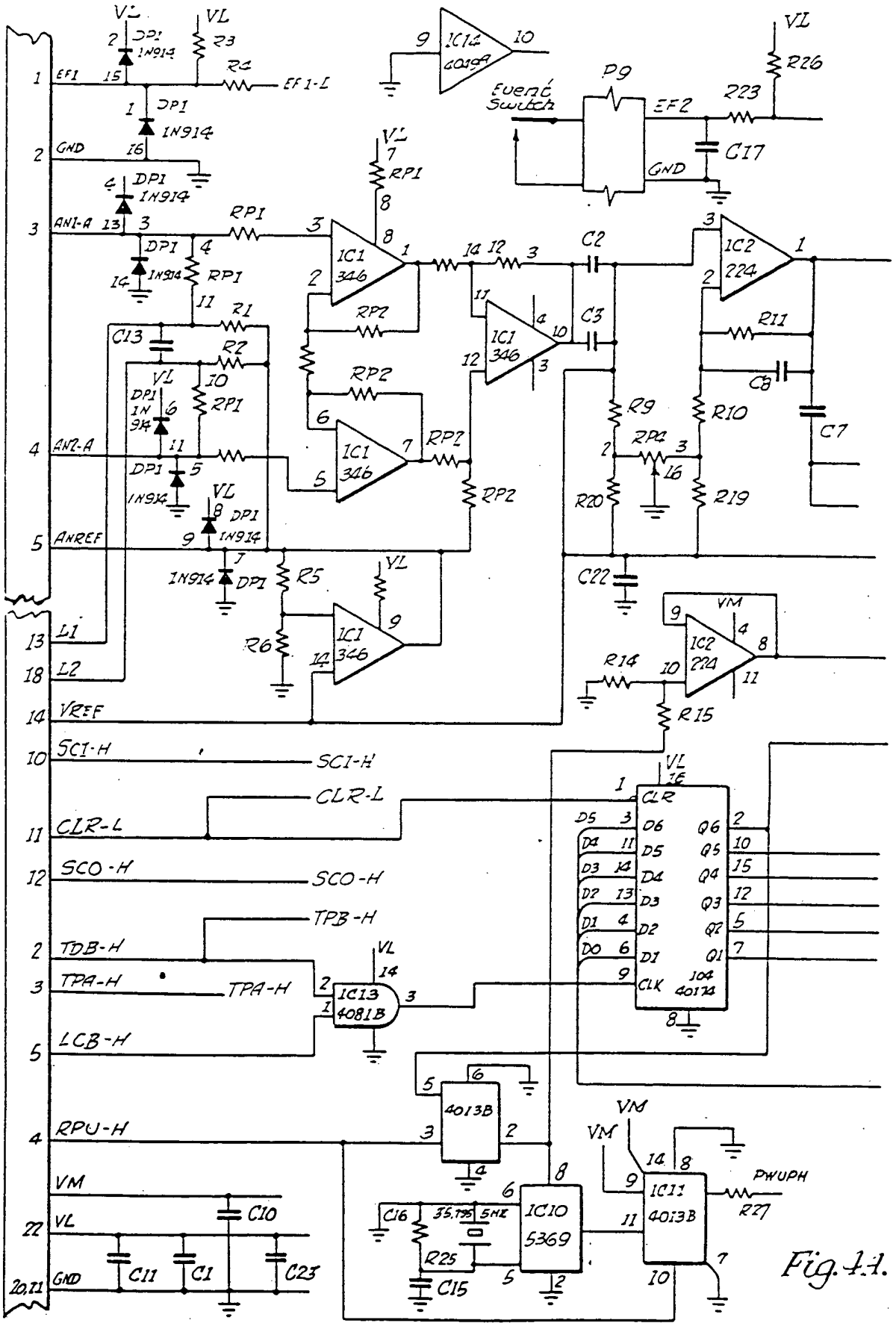
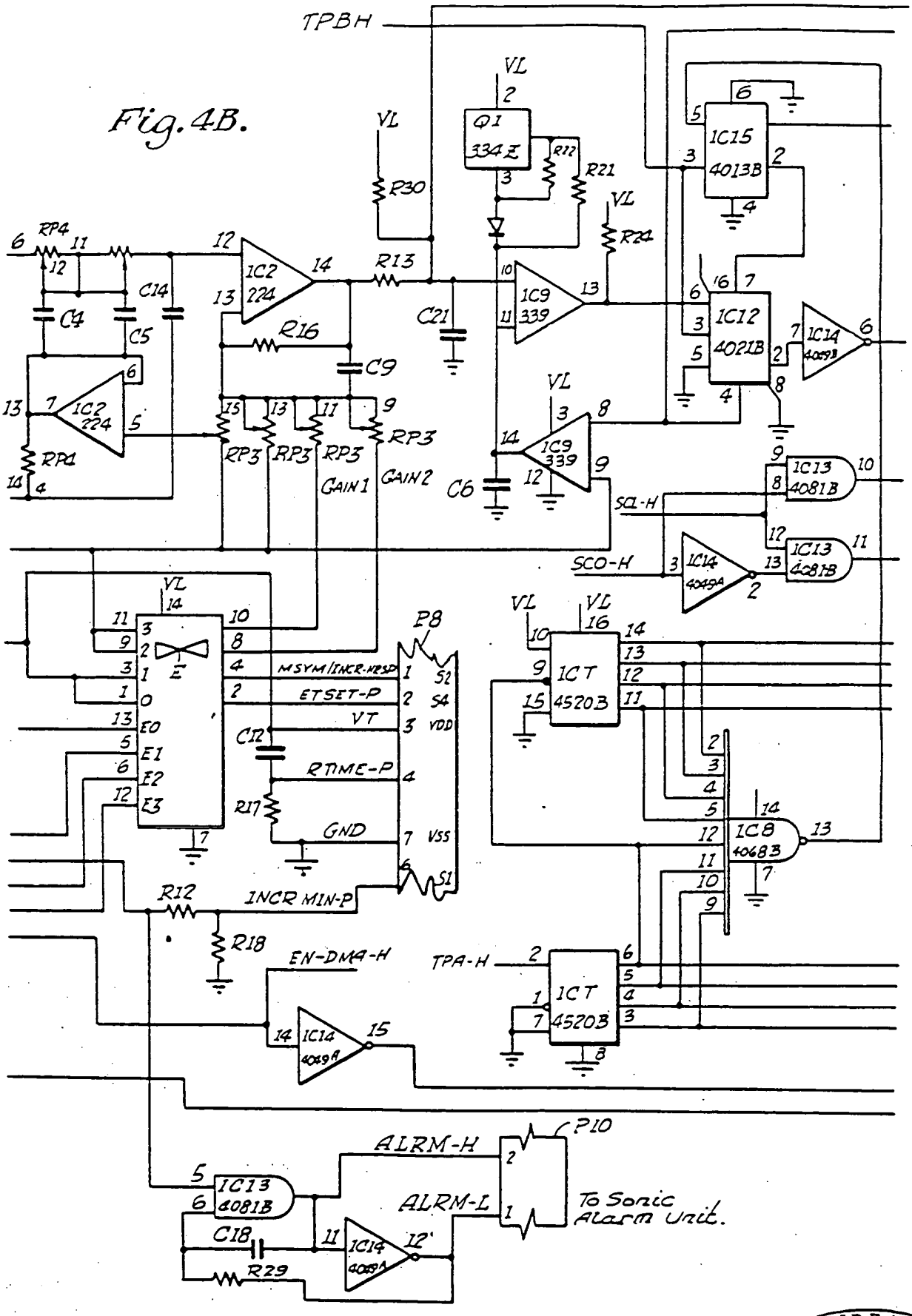


Fig. 11.

BUREAU

Fig. 4B.



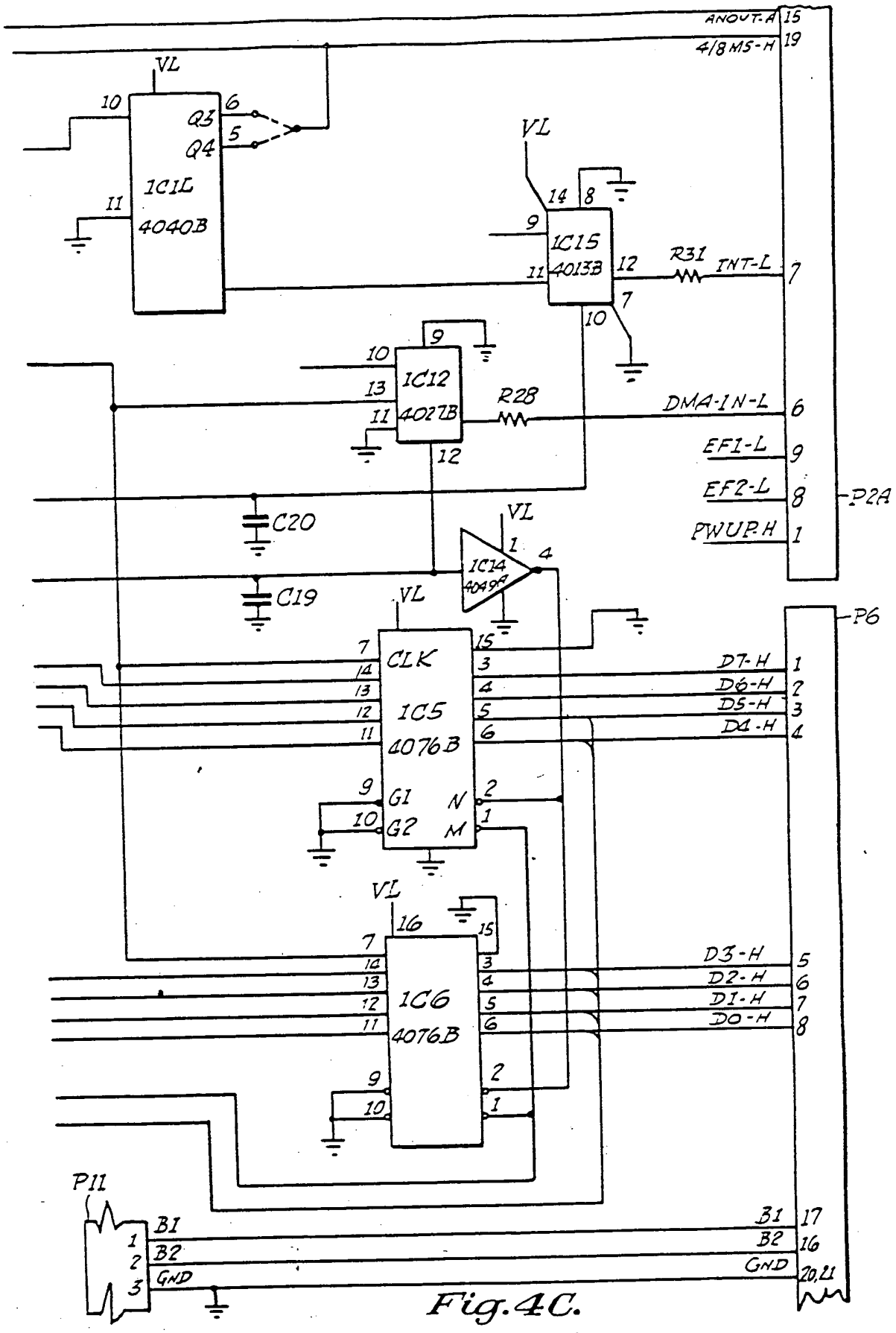


Fig. 4C.

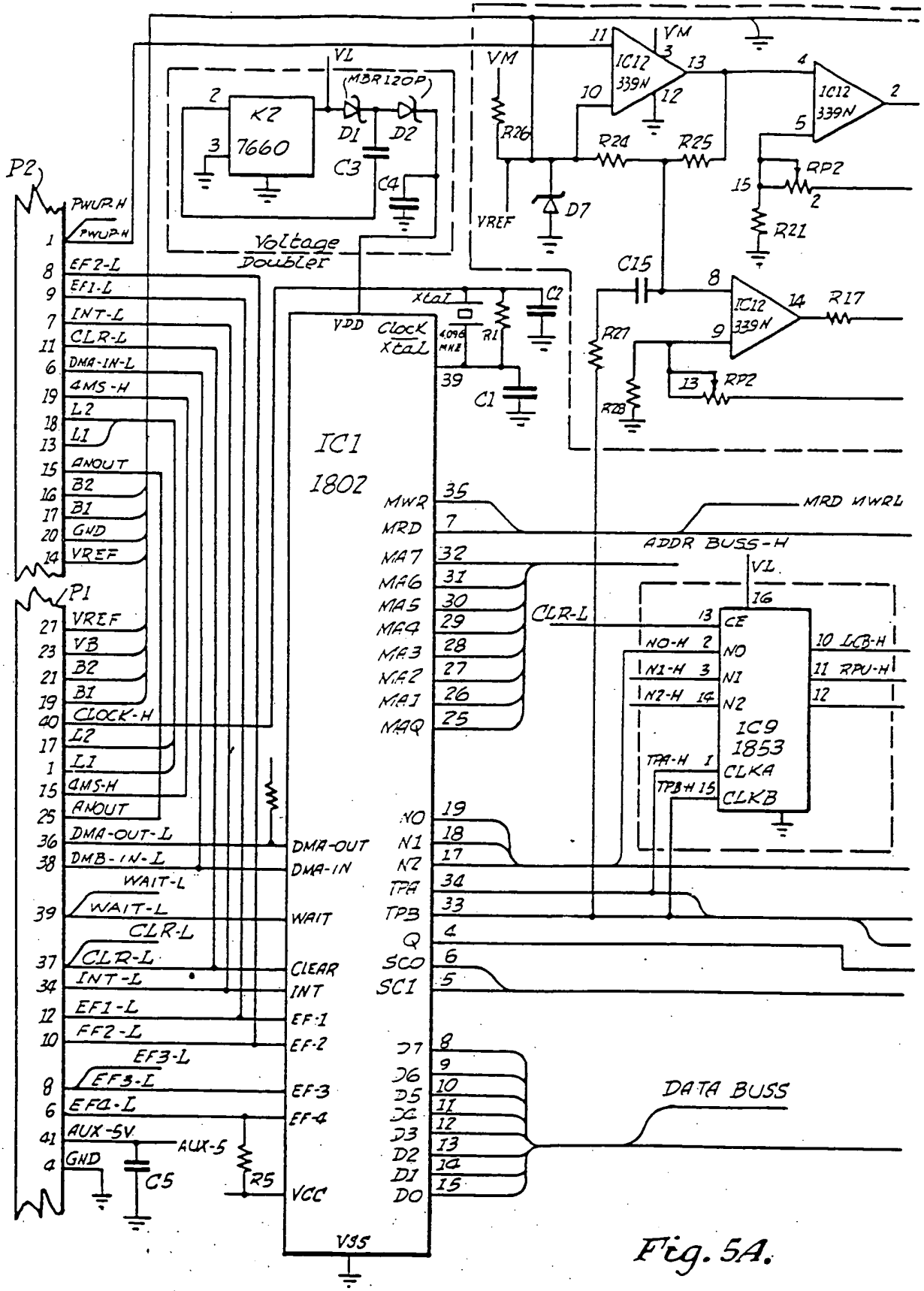


Fig. 5A.

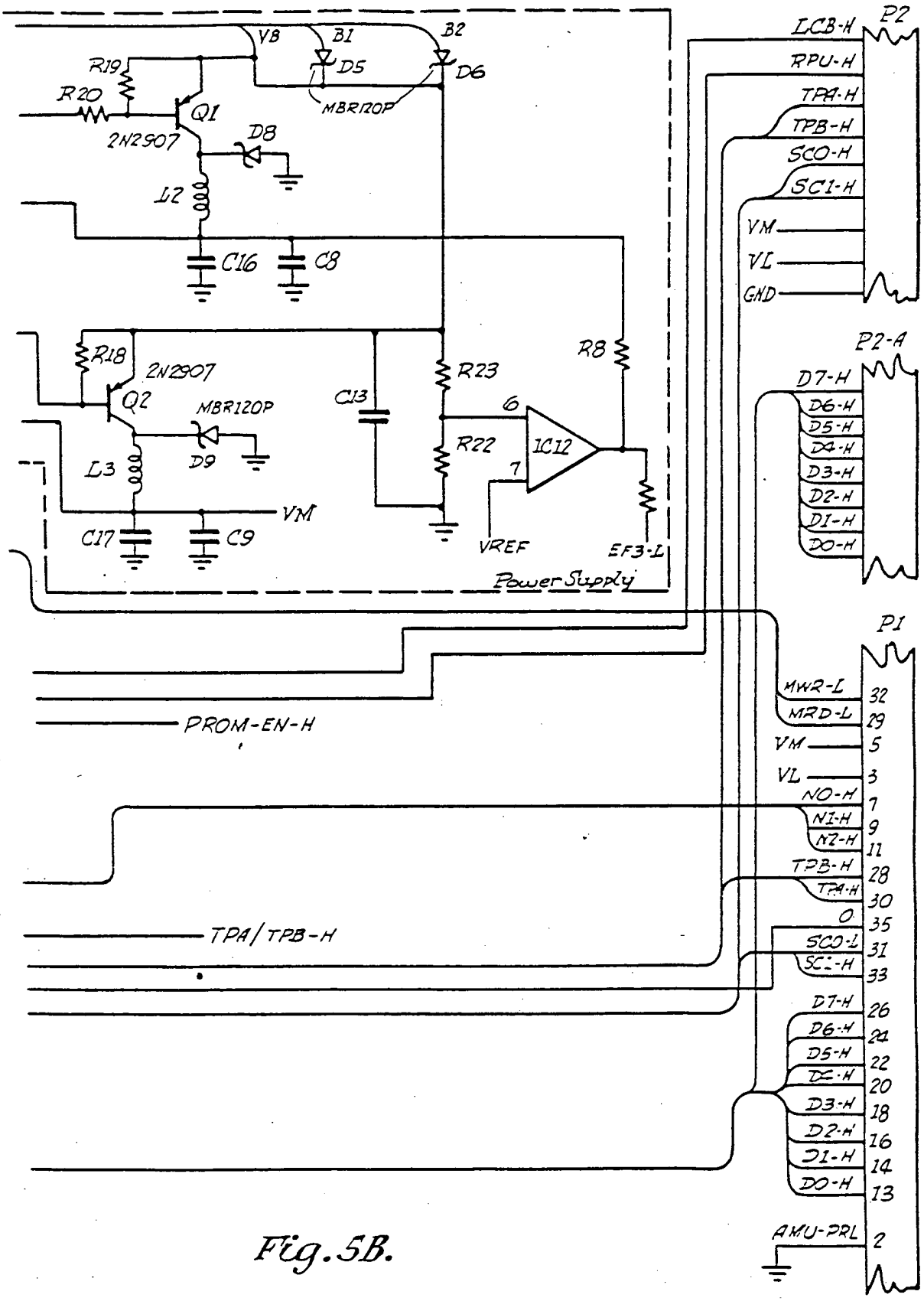


Fig. 5B.

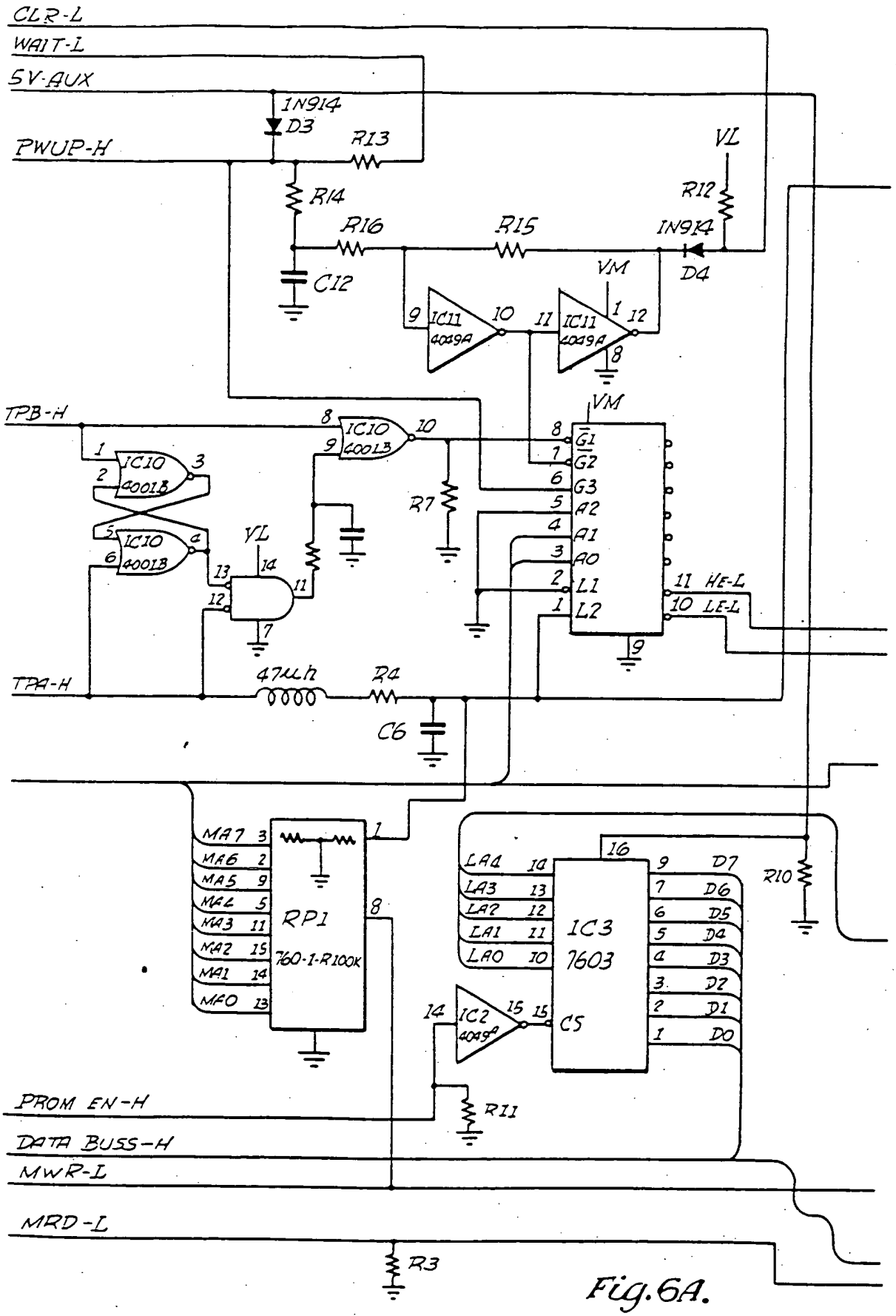


Fig. 6A.

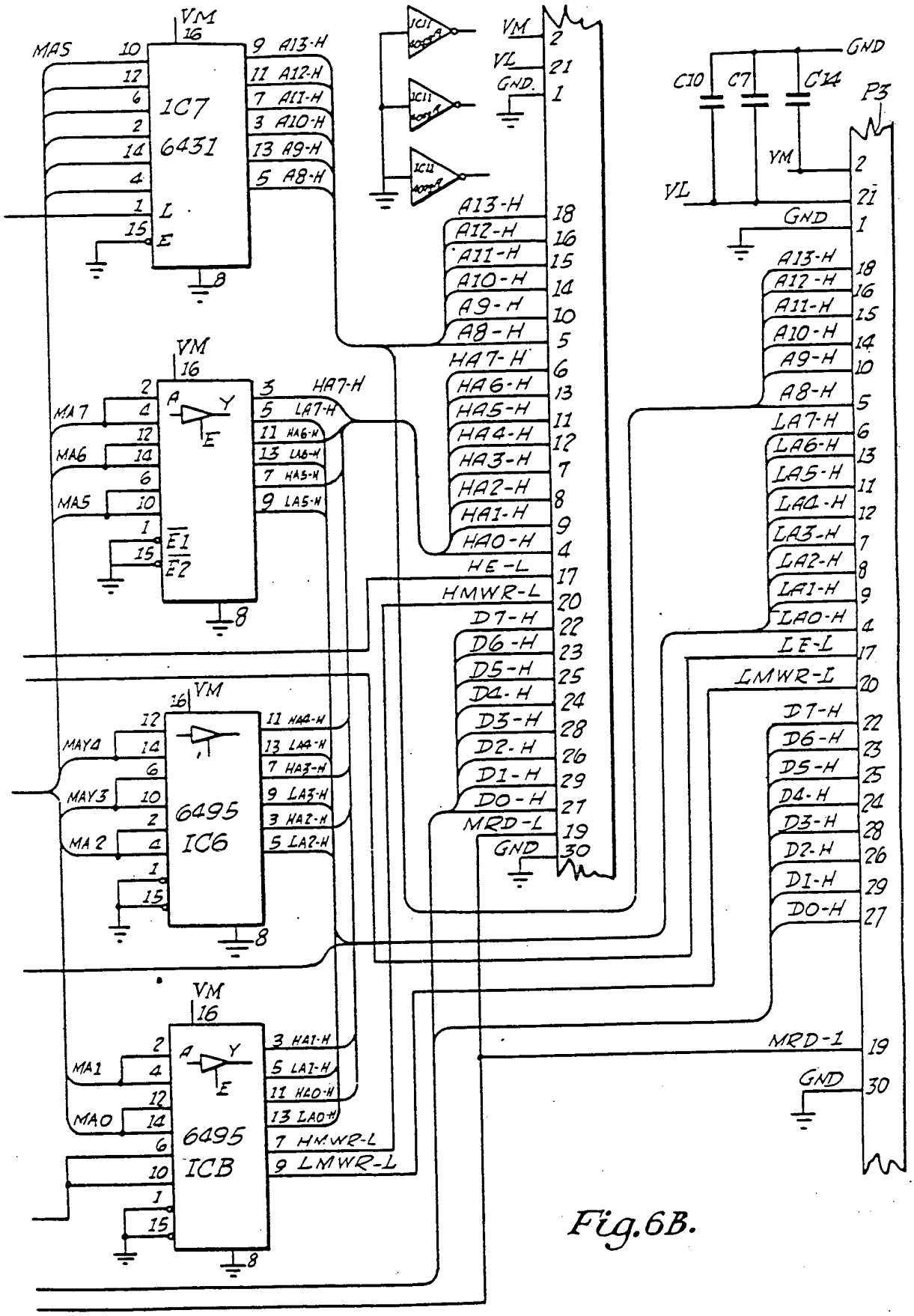


Fig.6B.

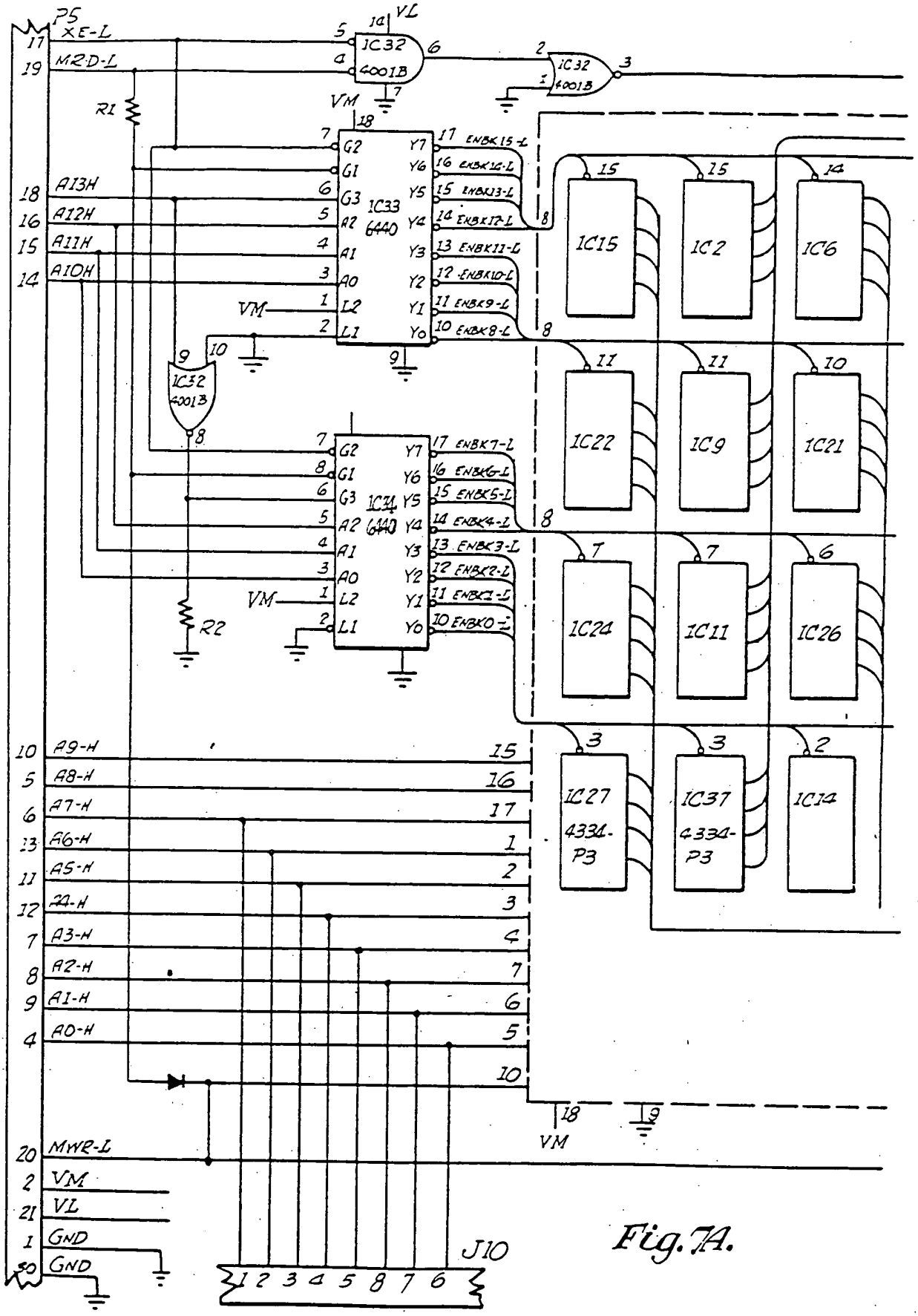


Fig. 7A.

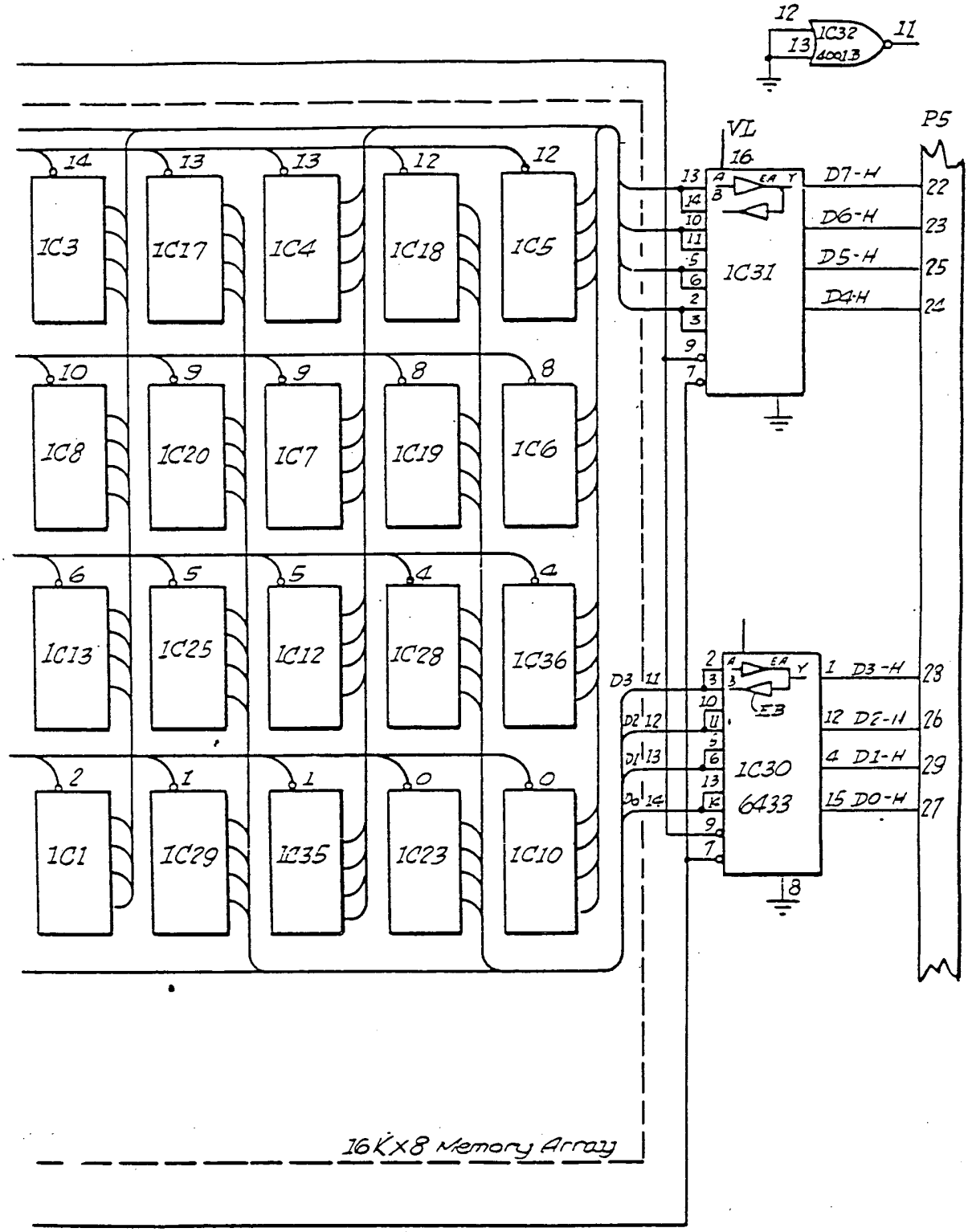
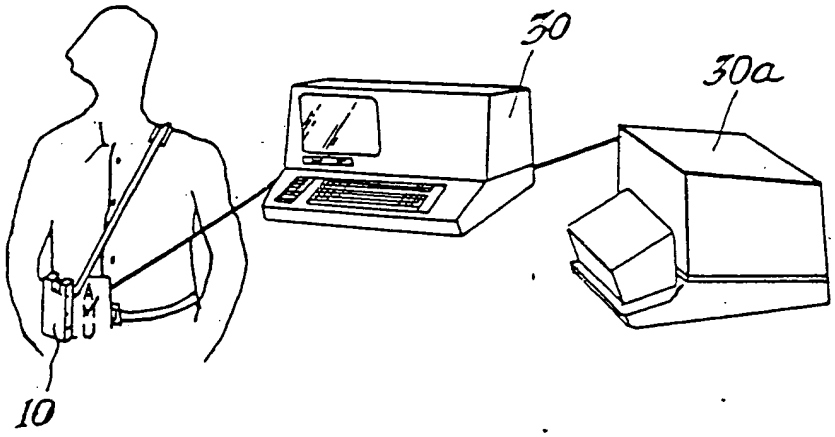


Fig. 7B.

Fig. 8A.



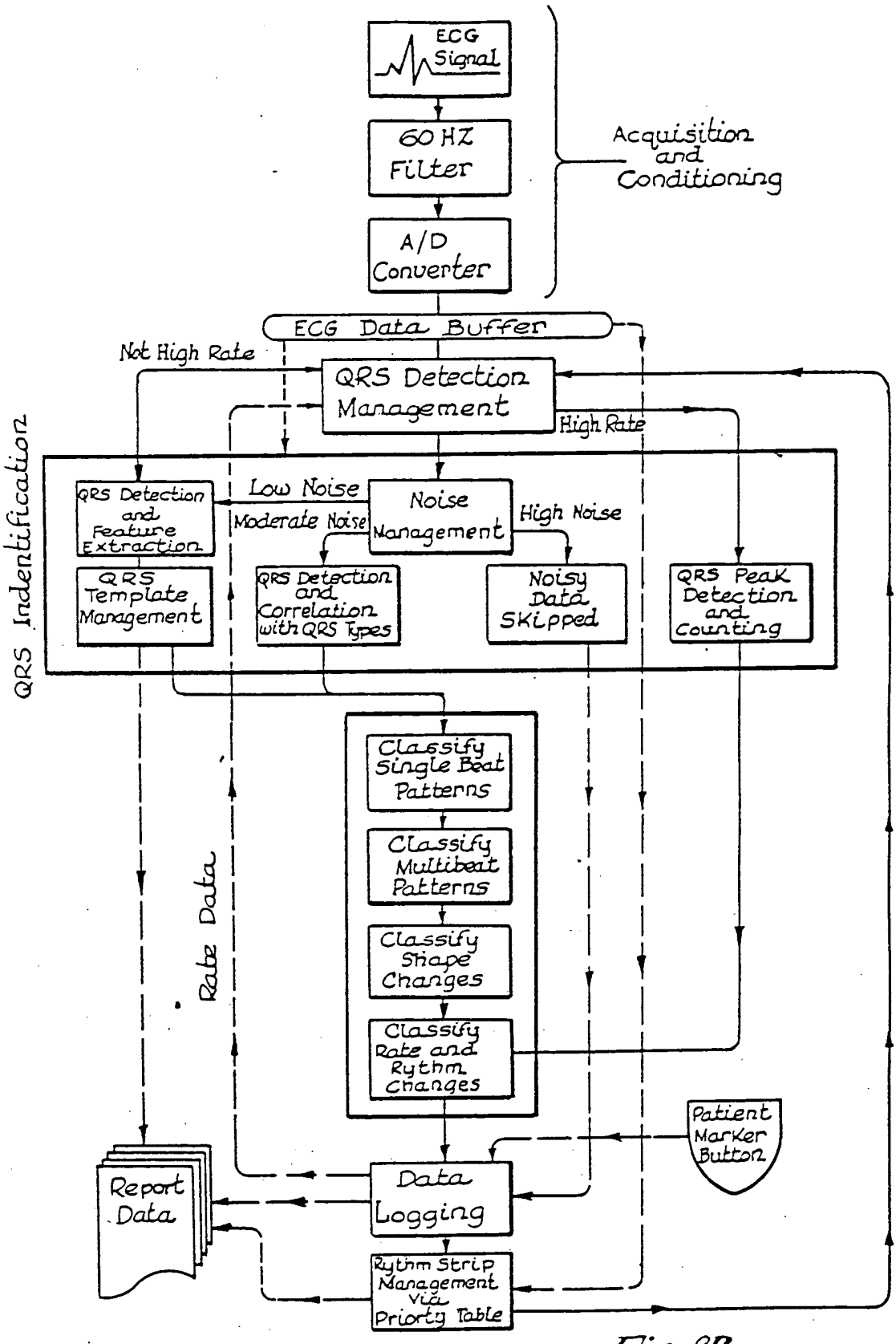

ECG Signal
60 HZ Filter
A/D Converter
Acquisition and Conditioning
ECG Data Buffer
Not High Rate
QRS Detection Management
High Rate
QRS Identification
QRS Detection and Feature Extraction
Low Noise
Moderate Noise
Noise Management
High Noise
QRS Template Management
QRS Detection and Correlation with QRS Types
Noisy Data Skipped
QRS Peak Detection and Counting
Classify Single Beat Patterns
Classify Multibeat Patterns
Classify Shape Changes
Classify Rate and Rythm Changes
Rate Data
Patient Marker Button
Report Data
Data Logging
Rythm Strip Management Via Priorty Table

Fig. 8B.

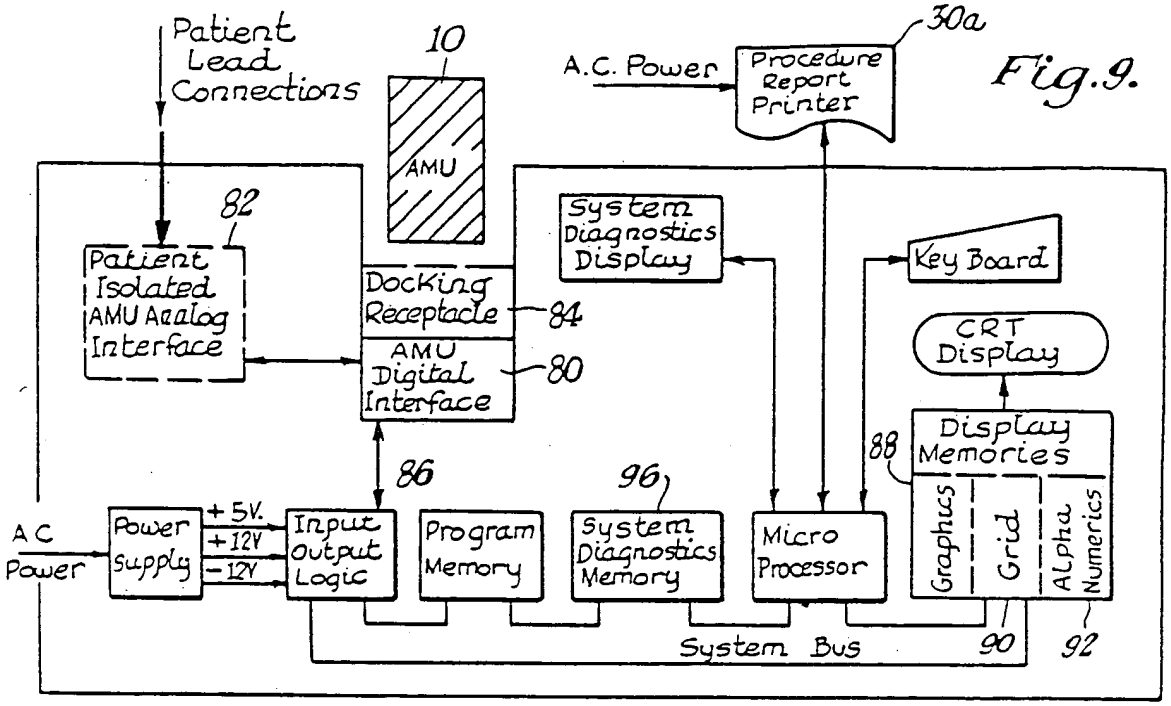


Fig.9.

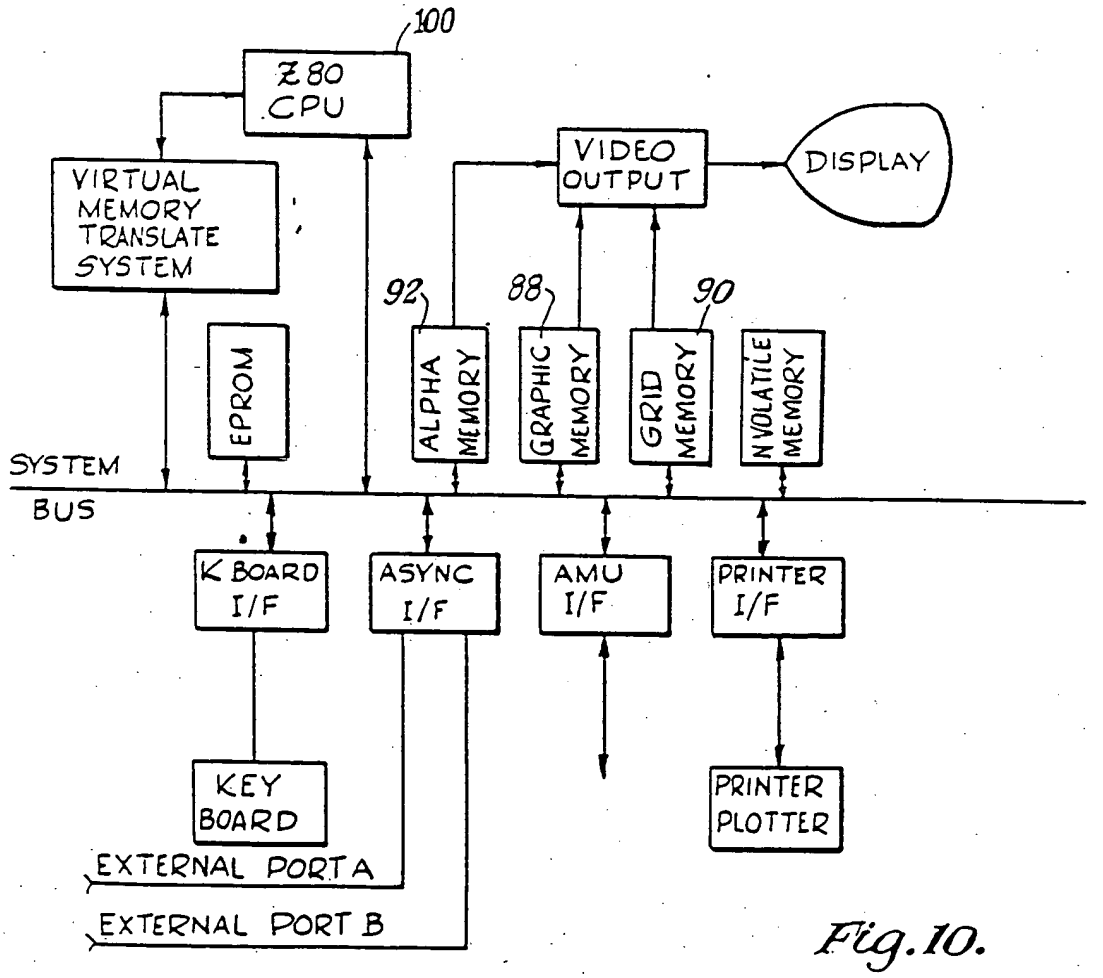


Fig.10.

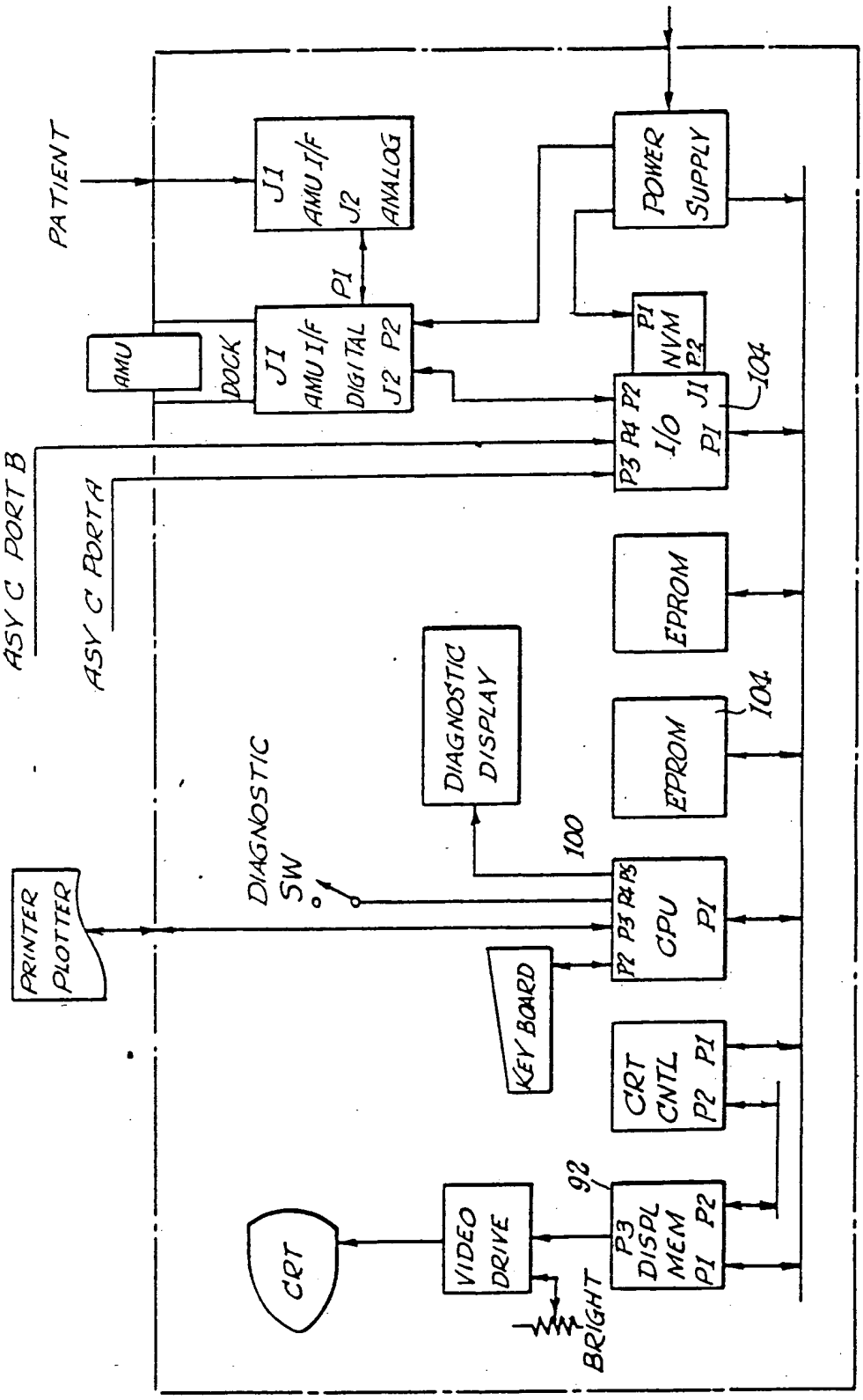


Fig. 10A.

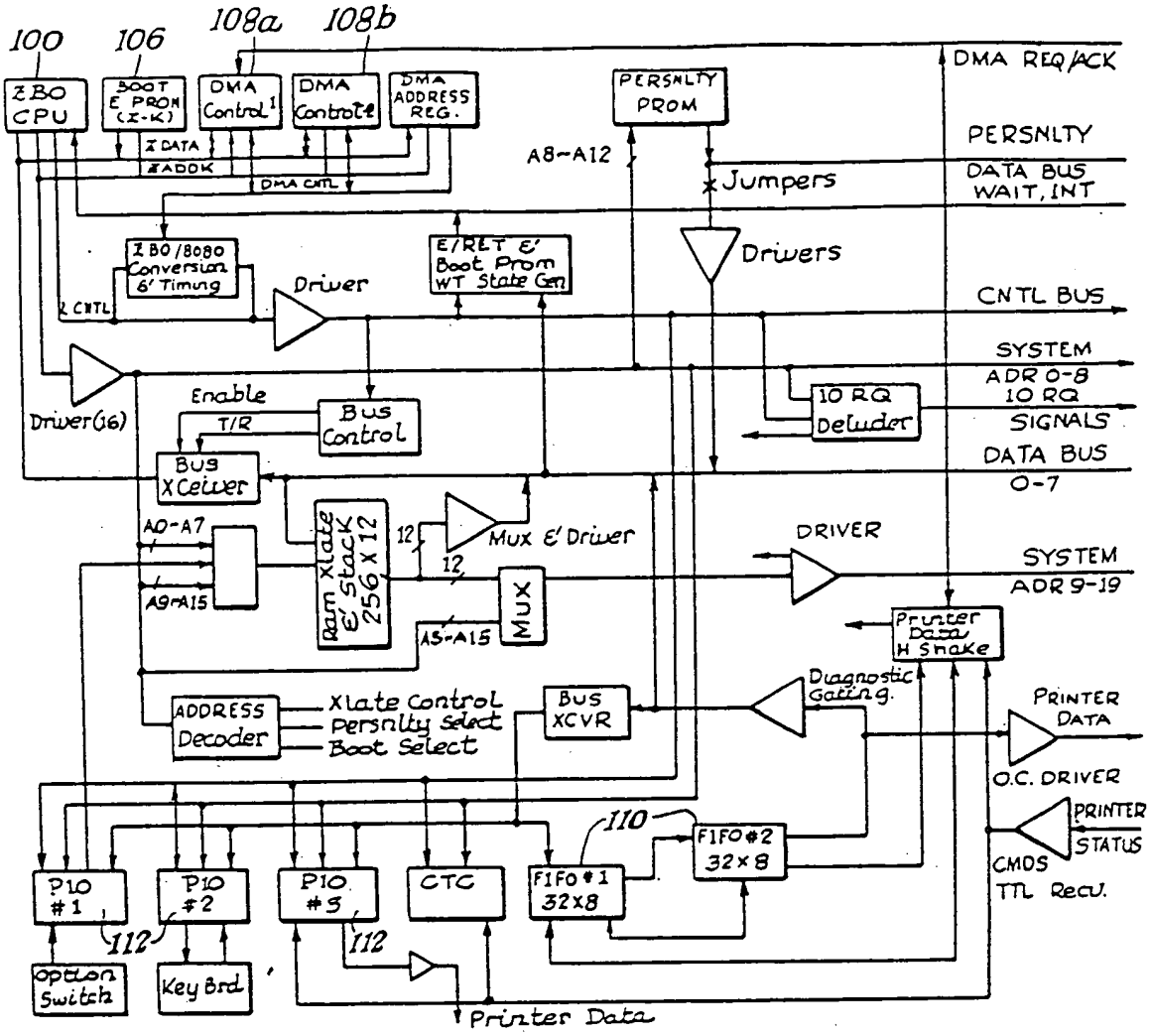


Fig.11A.

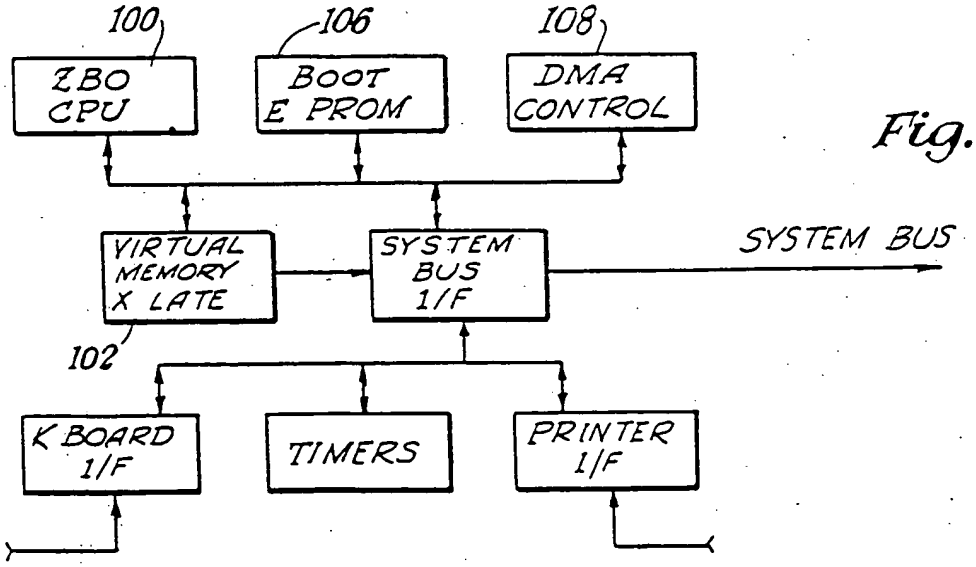


Fig. 11.

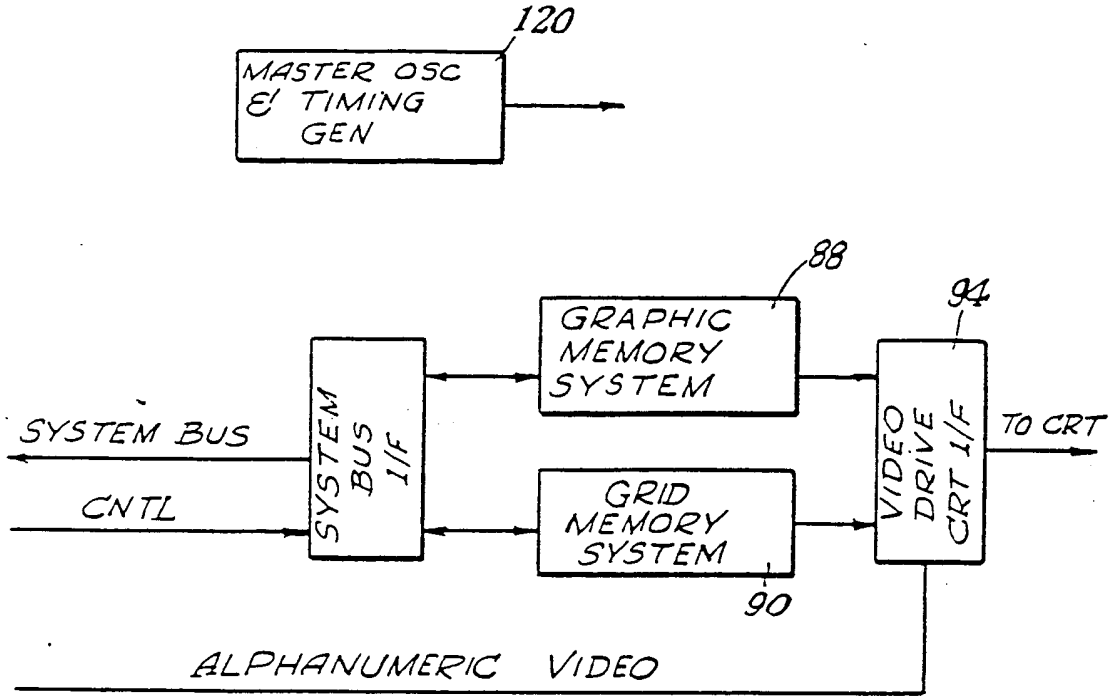


Fig. 12.

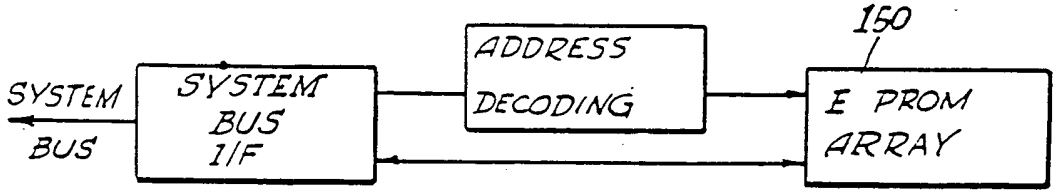


Fig. 14.

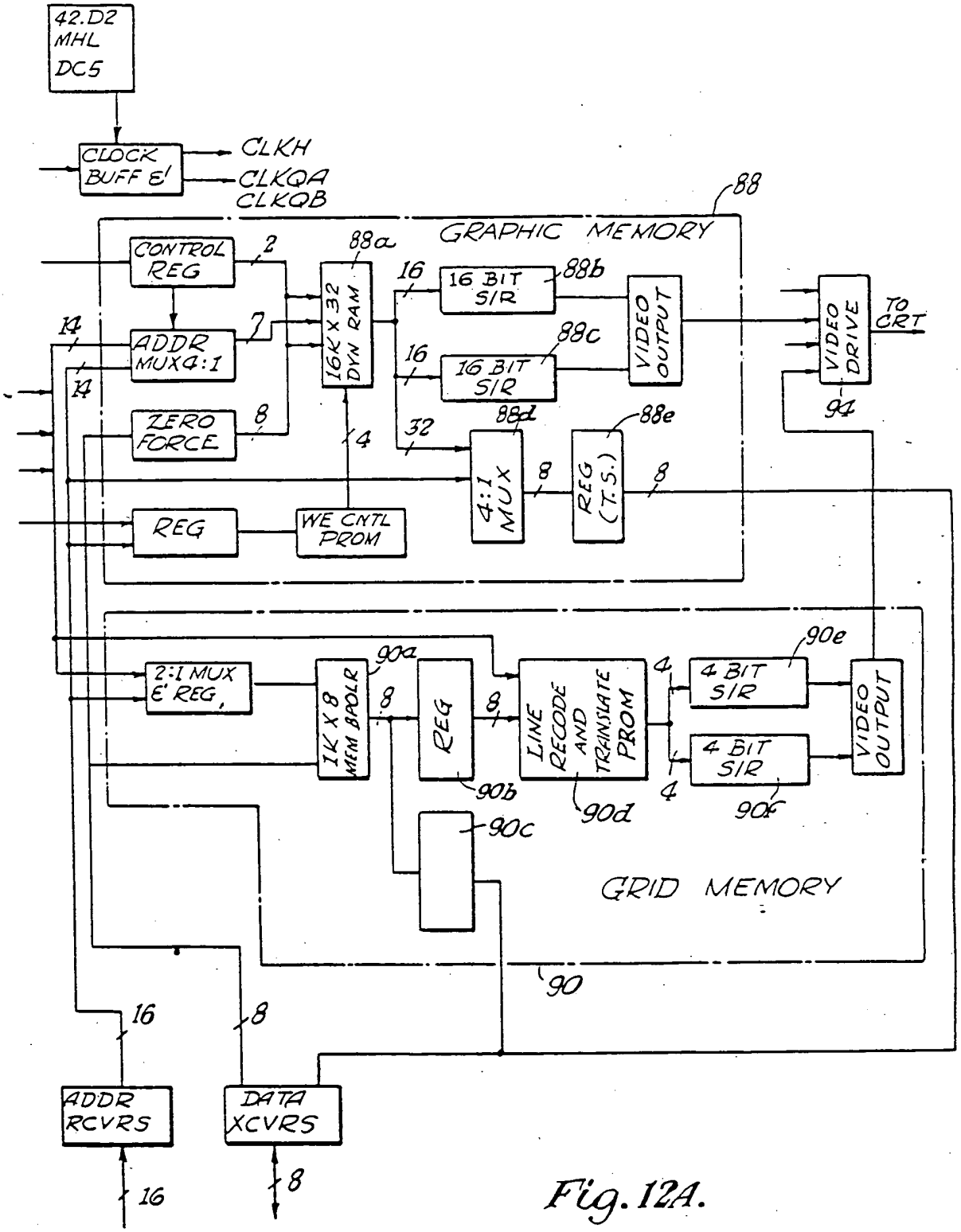

42.D2
MHL
DC5
CLOCK BUFF E'
CLKH
CLKQA
CLKQB
88
GRAPHIC MEMORY
CONTROL REG
2
88a
16
16 BIT S/R
88b
VIDEO OUTPUT
VIDEO DRIVE
TO CRT
14
ADDR MUX4:1
7
16K X 32 DYN RAM
16
16 BIT S/R
88c
14
ZERO FORCE
8
4
32
88d
4:1 MUX
88e
REG (T.S.)
8
8
94
REG
WE CNTL PROM
2:1 MUX E' REG,
90a
1K X 8 MEM BPOLR
8
REG
8
LINE RECODE AND TRANSLATE PROM
4
4 BIT S/R
90e
VIDEO OUTPUT
4 BIT S/R
4
90b
90d
90f
90c
GRID MEMORY
90
16
8
ADDR RCVRS
DATA XCVRS
16
8

Fig. 12A.

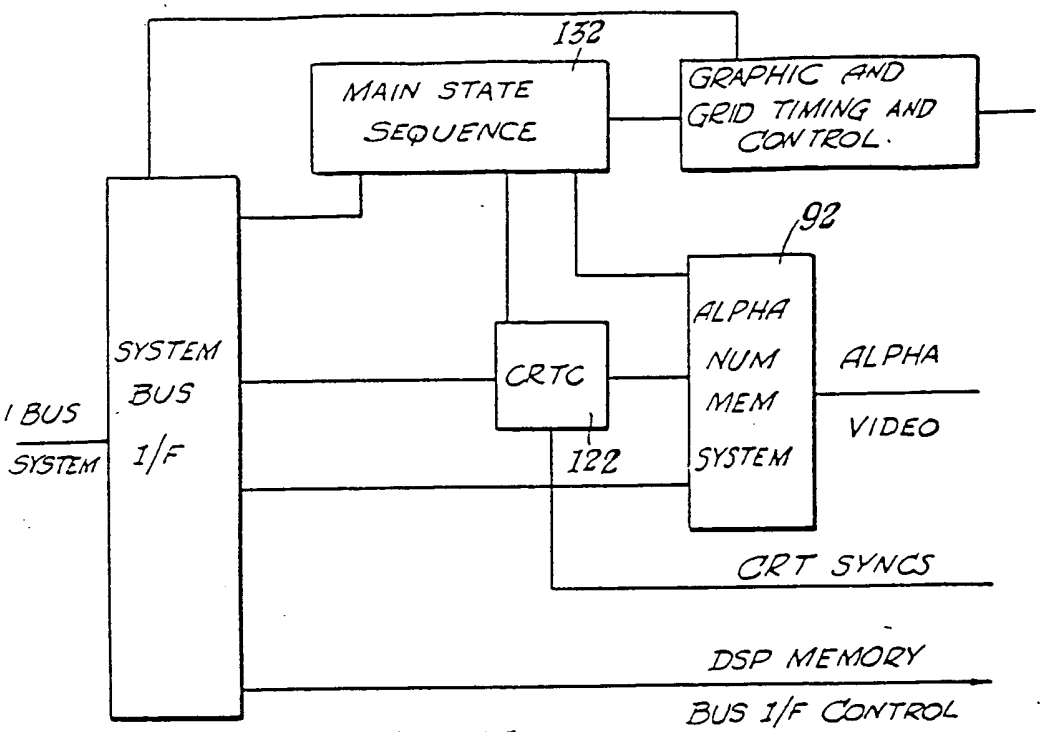
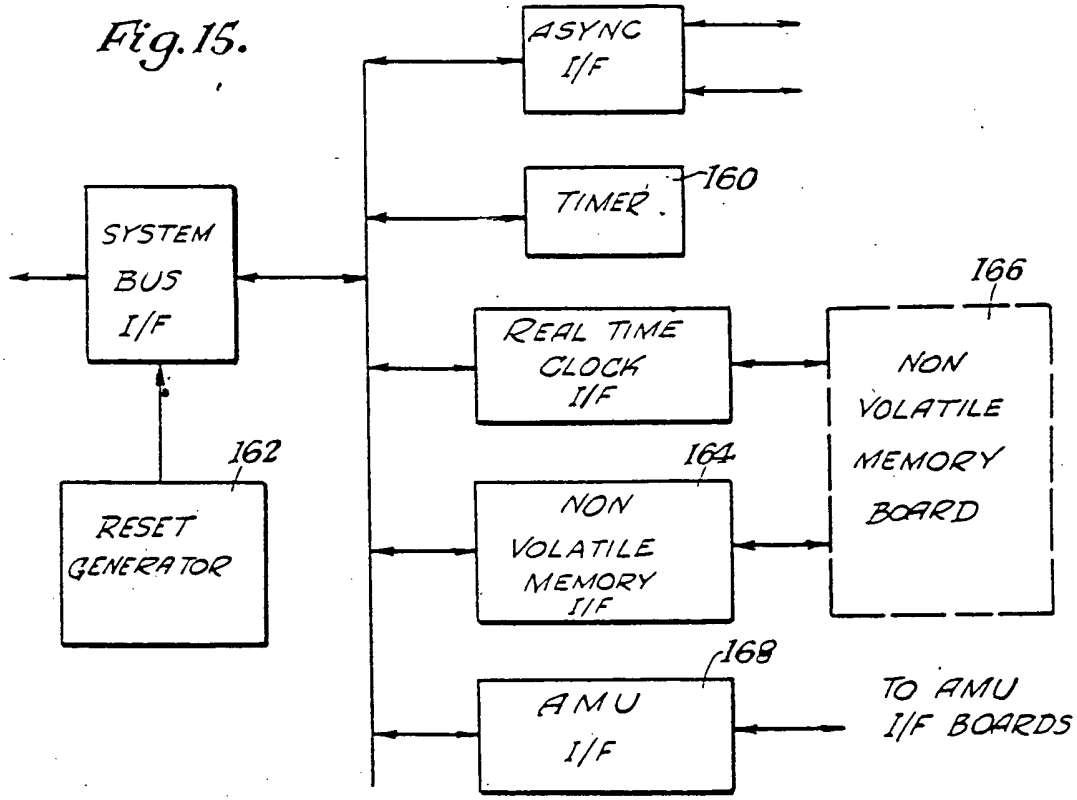


Fig. 13.

Fig. 15.



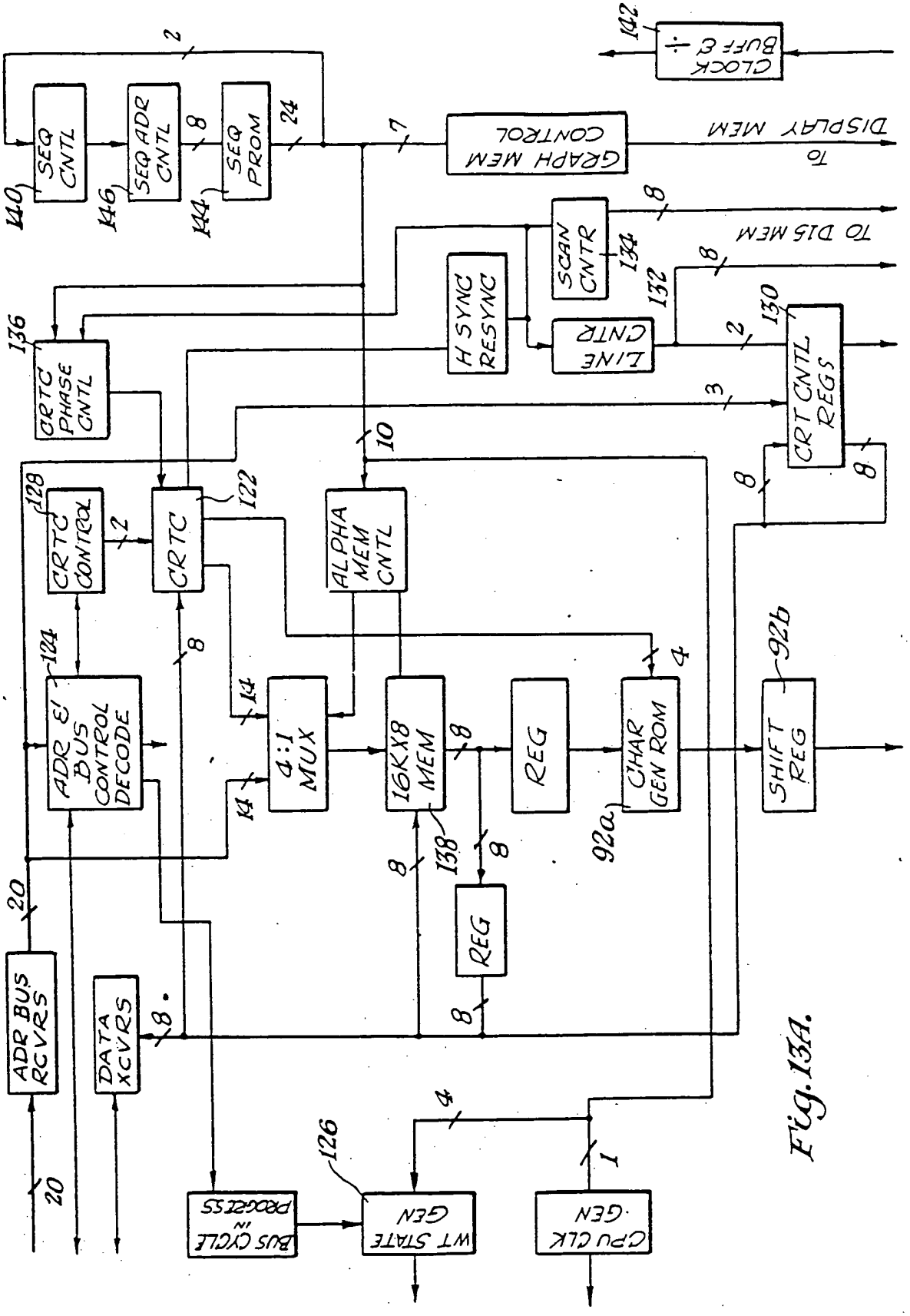


Fig. 13A.

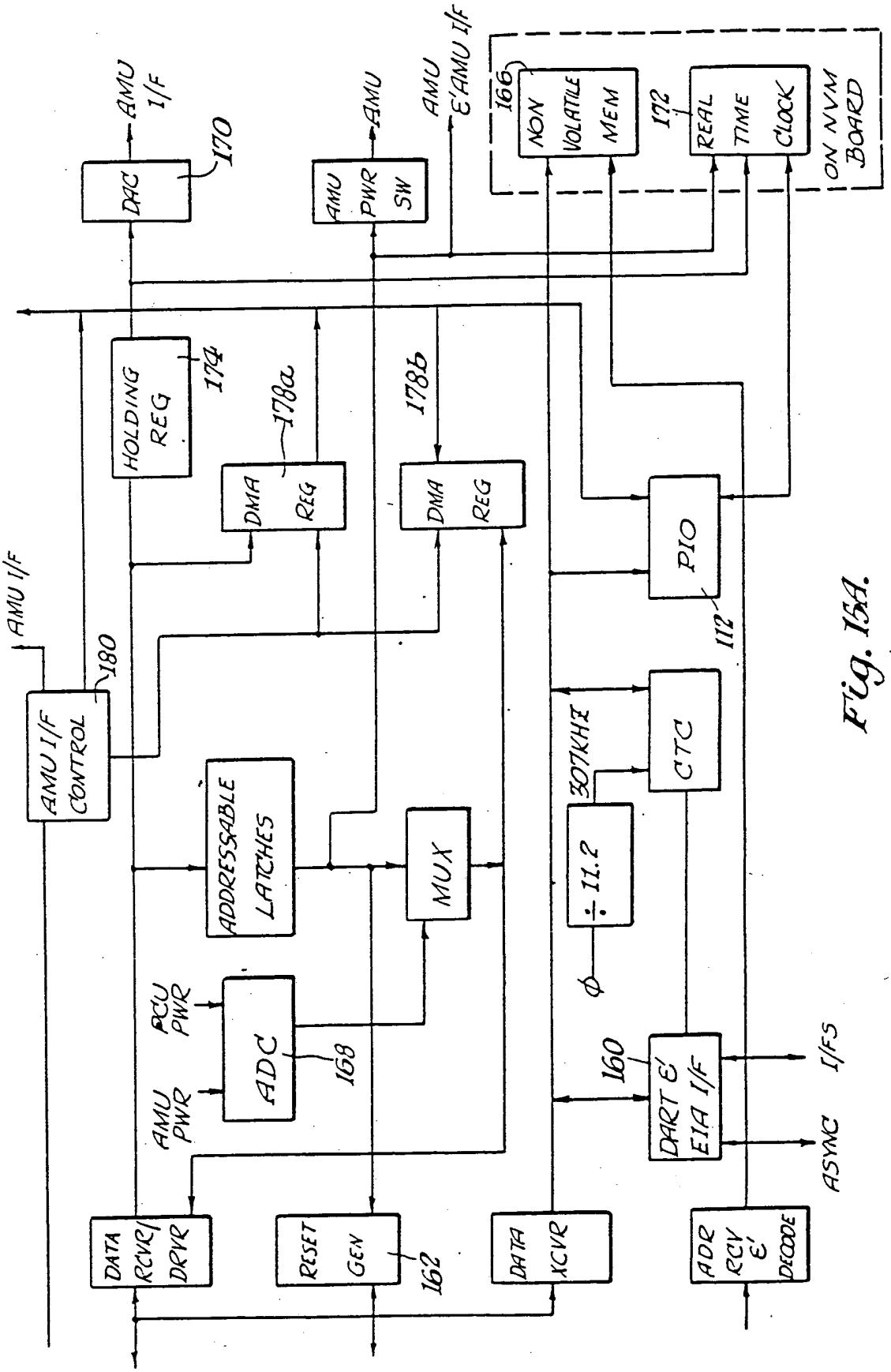


Fig. 15A.

Ambulatory Monitoring
and Analysis Report

5 Feb 81

Patient: (NAME)

Age: 86

Physician: Mt. Sinai Hospital EKG Lab
Procedure: ----- DATAMEDIX Standard -----

PCU Number: 5002400001 020108

AMU Number: 5002850023 000013

Procedure Duration: 22 Hours, 44 Minutes
Begun: 4 Feb 81 11:20 AM

Ended: 5 Feb 81 10:04 AM

Procedure Summary:

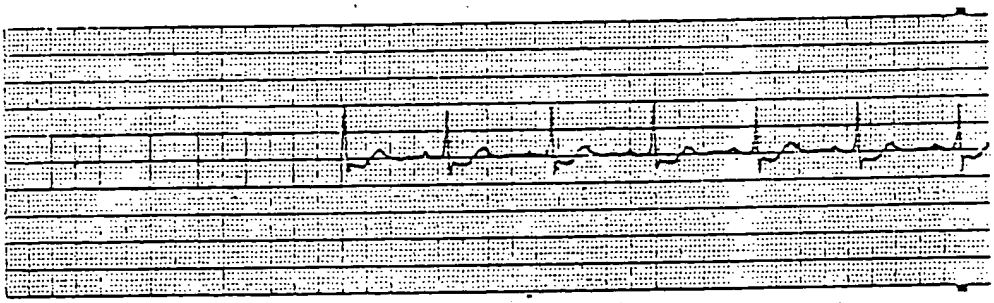
Total QRS Complexes Observed:	104747	Minimum Observed Rate:	60
Distinct QRS Types Observed:	6	Average Observed Rate:	79
Major QRS Pattern Changes Observed:	2	Maximum Observed Rate:	139
ECG Rhythm Strips Recorded:	24	Summary Period:	10 Minutes

Reference ECG:

Sensitivity: 0.1 Millivolts per Division
Time Scale: 5 Major Divisions per Second

ECG Number 00
11:27:43 AM

QRS Width:
.088 Sec



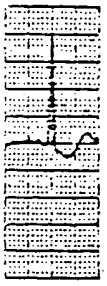
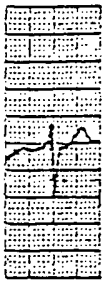
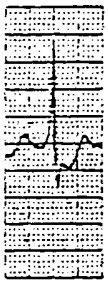
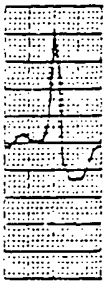
Specimen: 1 Millivolt Calibration, Typical QRS

Physician Review and Interpretation:

FIG.18A

Patient: 5 Feb 81

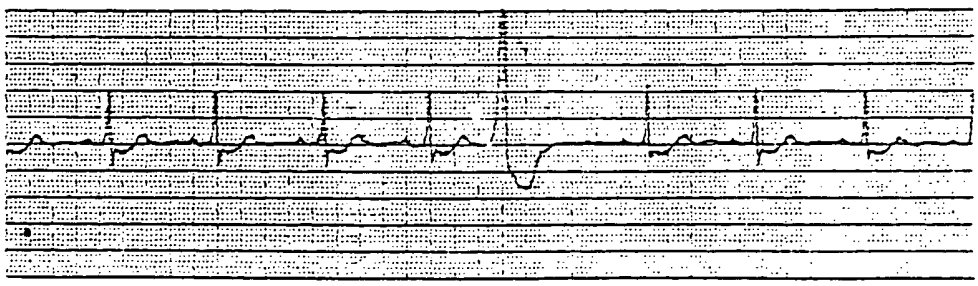
QRS Types:

Label:	T1	I1	I2	W1
				
Number				
Observed:	61249	75	2	79
Probable:	18	3	0	7

Label:	W2	W3
		
Number		
Observed:	19	42870
Probable:	0	99

ECG Rhythm Strips:

ECG Number 01
11:41:05 AM



Rate: 69 BPM
Rhythm: Reg.
QRS Width:
.092 Sec

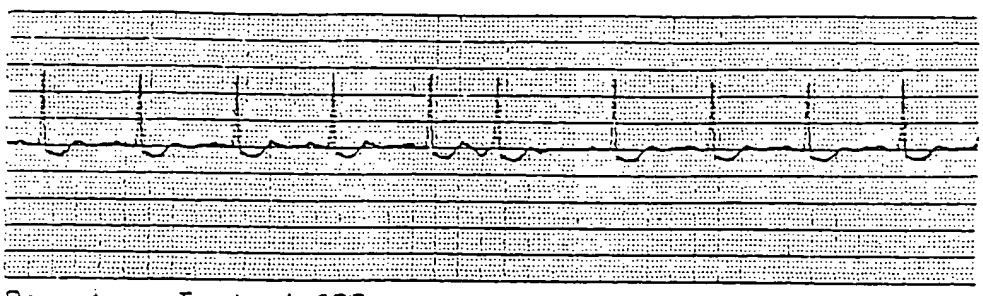
Specimen: Premature Atypical QRS

FIG.18B

Patient: 5 Feb 81

ECG Number 10
1:30:33 PM

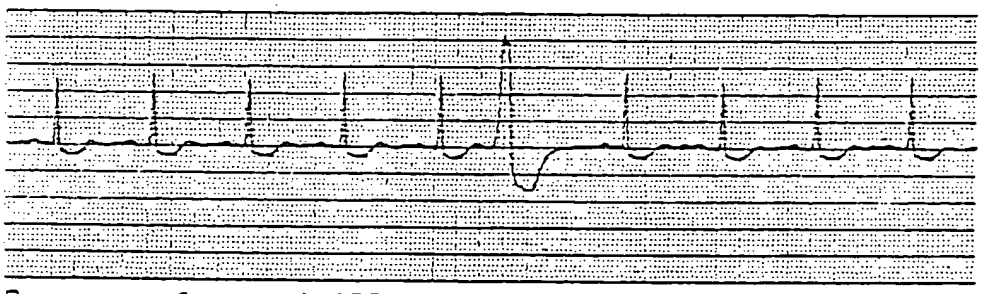
Rate: 77 BPM
Rhythm: Reg.
QRS Width:
.064 Sec



Specimen: Premature Typical QRS

ECG Number 11
1:35:40 PM

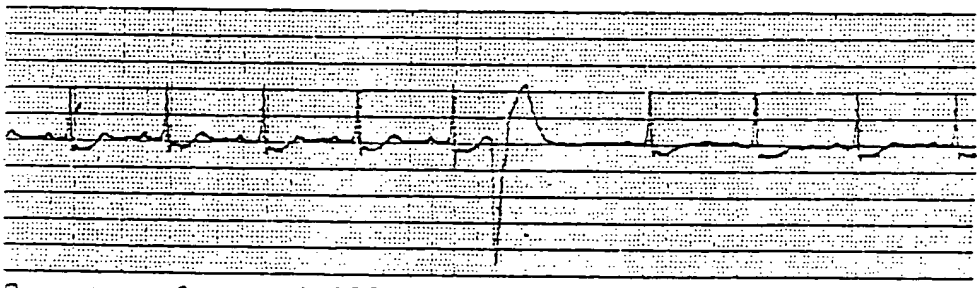
Rate: 79 BPM
Rhythm: Reg.
QRS Width:
.076 Sec



Specimen: Premature Atypical QRS

ECG Number 12
2:01:47 PM

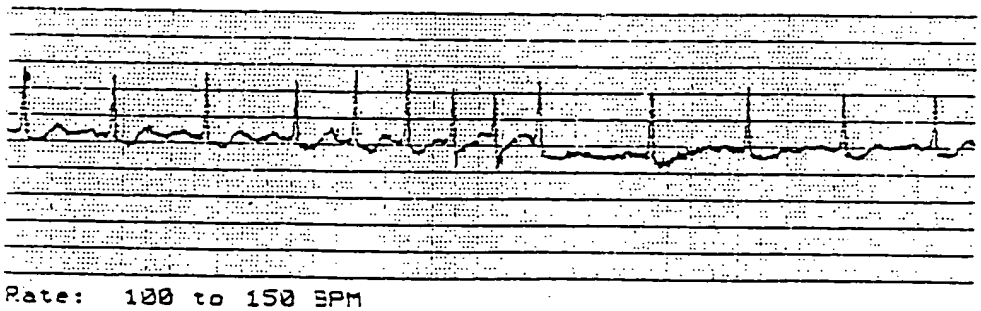
Rate: 80 BPM
Rhythm: Reg.
QRS Width:
.080 Sec



Specimen: Premature Atypical QRS

ECG Number 13
9:10:03 PM

Rate: 101 BPM
Rhythm: Reg.
QRS Width:
.068 Sec



Specimen: Rate: 100 to 150 BPM

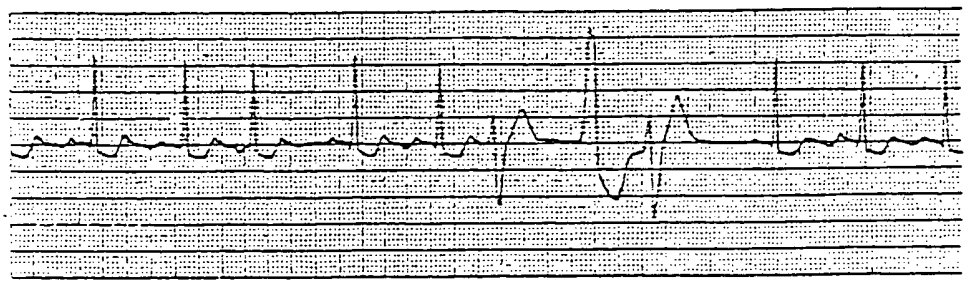
FIG. 18C-1

Patient: Samuel Rose 5 Feb 81 Page 7

ECG Rhythm Strips (continued) :

ECG Number 18
5:12:56 AM

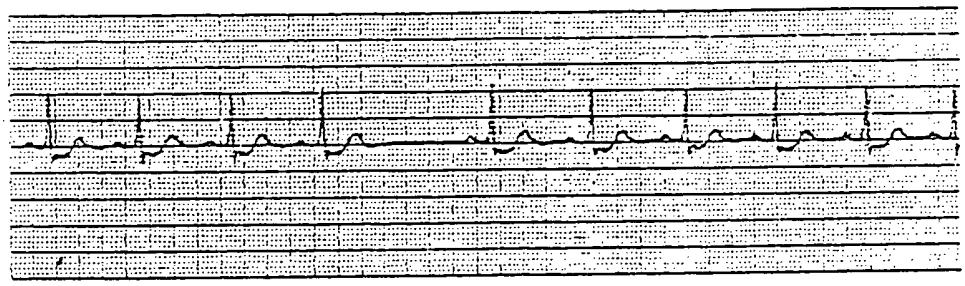
Rate: 84 BPM
Rhythm: Reg.
QRS Width:
.076 Sec



Specimen: Triplet, Atypical QRS

ECG Number 24
9:42:15 AM

Rate: 70 BPM
Rhythm: Reg.
QRS Width:
.076 Sec



Specimen: Missed Beat(s)

FIG.18C-2

Patient: 5 Feb 81

Phenomena Summary:

QRS Rate -- 8 Beat Average

Bradycardia at Rates:
between 50 and 60 BPM

Normal at Rates between 60 and 100 BPM

Tachycardia at Rates:
between 100 and 150 BPM

Single QRS Shape and R-R Interval

461 Premature Typical QRS Complexes
20 Occurred at a Rate of 6/Minute or Greater

225 Premature Atypical QRS Complexes

13 Pause(s)

3 Missed Beat(s)

QRS Sequences

1 Episodes of Bigeminy with Typical QRS Complexes

5 Episodes of Bigeminy with Atypical QRS Complexes

5 Episodes of Couplets with Atypical QRS Complexes

1 Episodes of Triplets with Atypical QRS Complexes

Major QRS Pattern Changes

2 Episodes of Major Pattern Changes in QRS Complexes

Major QRS Pattern Change Log:

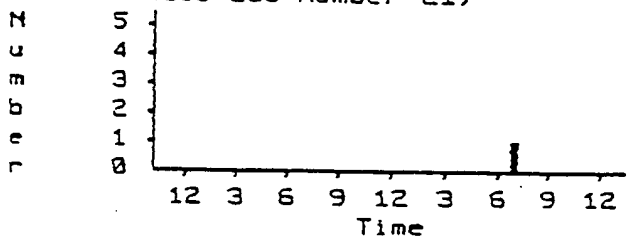
Log Number	Onset Time of Day	Duration in Secs.	Rate (BPM) Bef	Rate (BPM) Aft	Rhythm Bef	Rhythm Aft	Width (Ms) Bef	Width (Ms) Aft	ECG Number
1	4:37:58 AM		84 **	128	Reg	Reg	64	68	
2	4:39:08 AM		135 **	76	Reg	Reg	68	72	

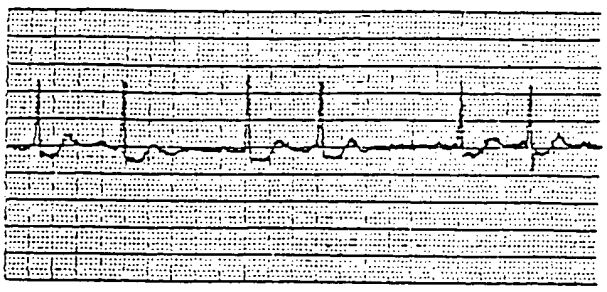
FIG.18D

Patient: 5 Feb 81

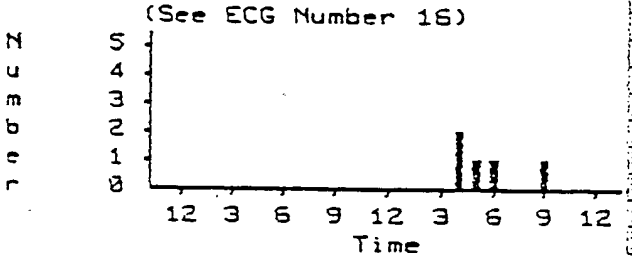
Hourly Summaries:

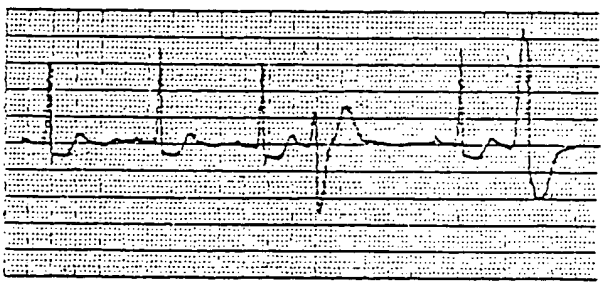
Bigeminy, Typical QRS Total 1
(See ECG Number 21)



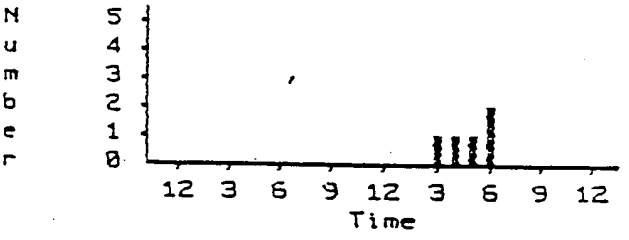


Bigeminy, Atypical QRS Total 5
(See ECG Number 16)



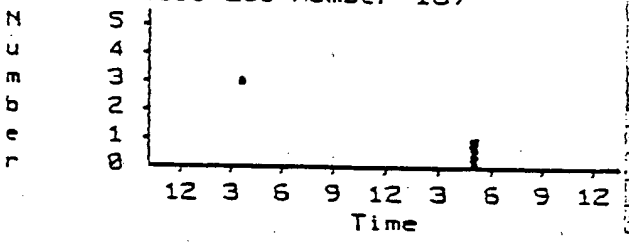


Couplet, Atypical QRS Total 5



(No ECG Rhythm Strip Available)

Triplet, Atypical QRS Total 1
(See ECG Number 18)



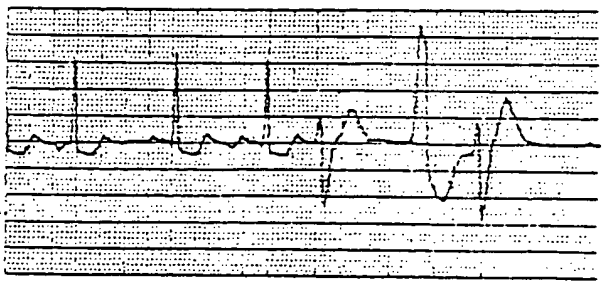
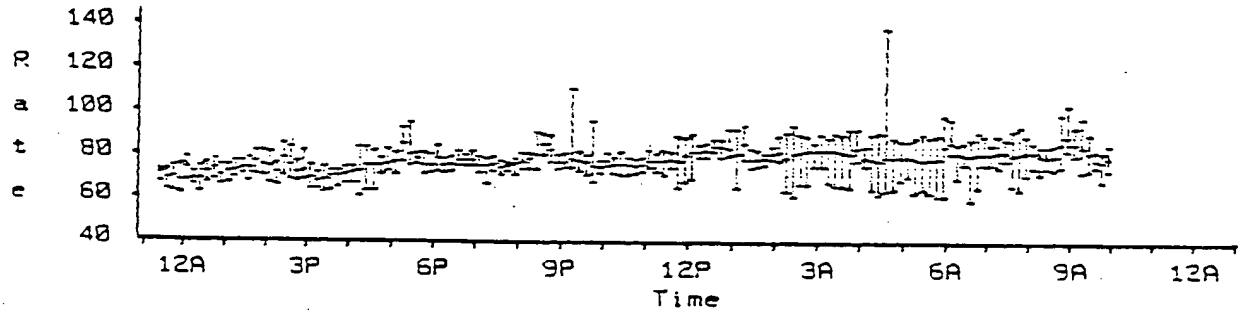


FIG. 18E

Patient: 5 Feb 81

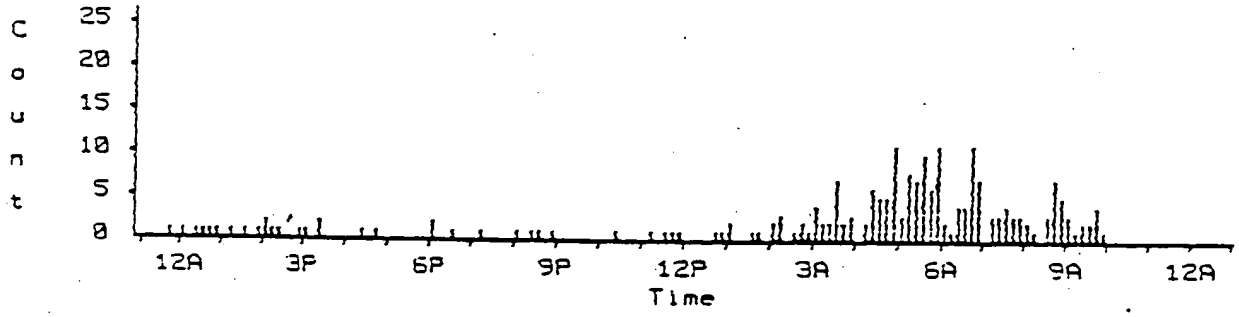
Rate Summary

Maximum Average Minimum



Premeture Atupical QRS Summary

Count per 10 Minutes
(* = Rate > 6 per Minute)



Premature Tupical QRS Summary

Count per 10 Minutes
(* = Rate > 6 per Minute)

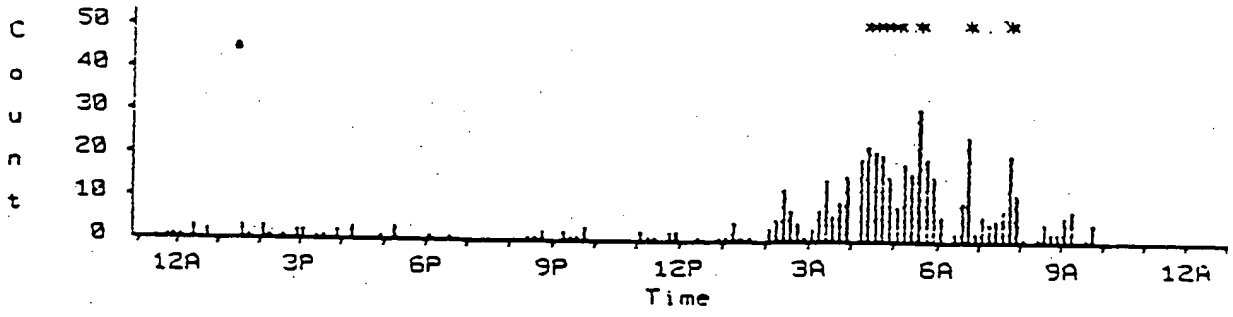
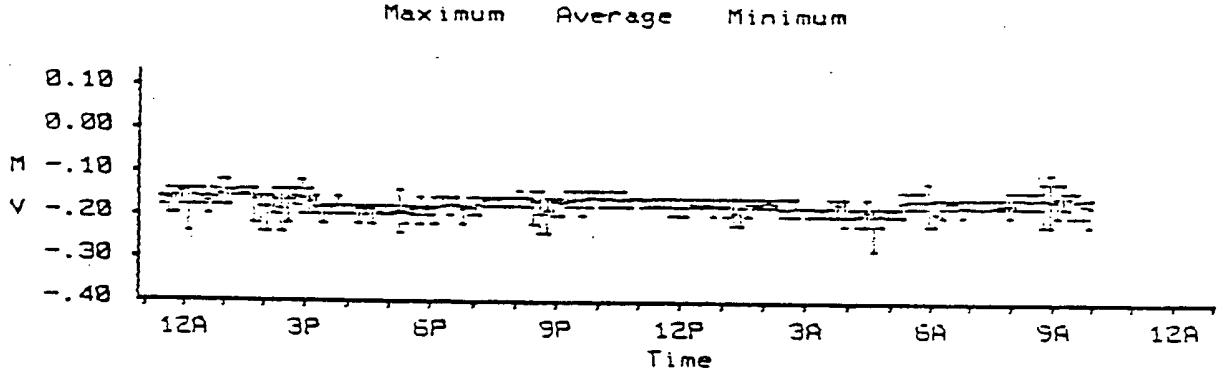


FIG.18F

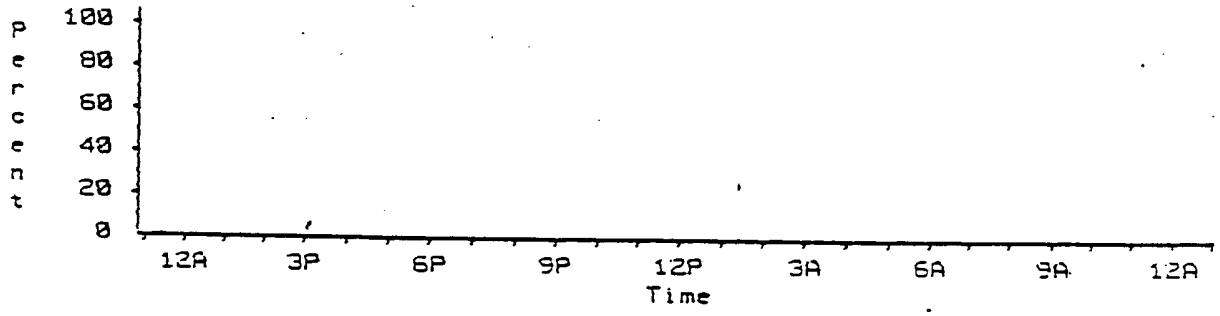
Patient: 5 Feb 81

S-T Deflection Summary



Noise/Artifact

Percent of Summary Period Loss Due to Noise or Artifact



Loss of Sustem Function

Percent of Summary Period Loss Due to Disconnected Leads

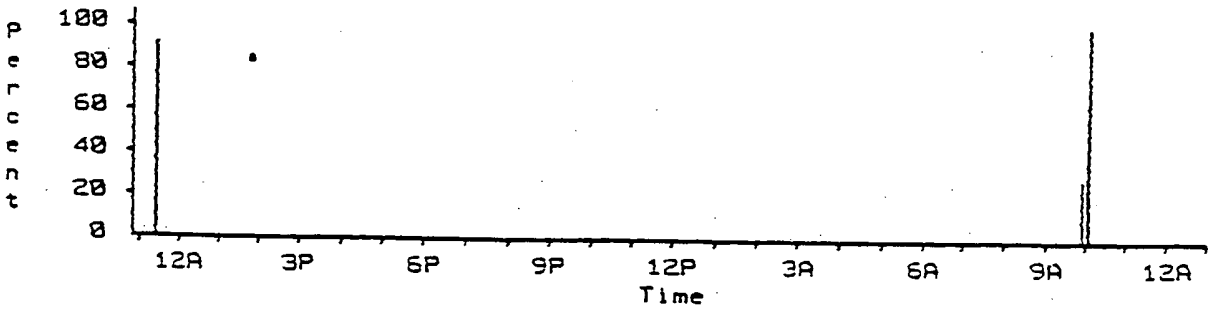


FIG.18G

Patient: 5 Feb 81

Summary Period Log:

Start Time HH:MM	Rate Min (BPM)	Rate Avg (BPM)	Rate Max (BPM)	Prem Atyp QRS	Prem Typ QRS	S-T Deflection Min (Millivolts)	S-T Deflection Avg (Millivolts)	S-T Deflection Max (Millivolts)	# of Rhym Strp	# of Majr Ptrn	Noise /Artl MM:SS	Lead-less MM:SS
11:20	66	71	73	0	0	-.18	-.18	-.16	0	0	0:03	9:03
11:30	63	69	72	0	0	-.20	-.18	-.14	0	0	0:00	0:00
11:40	63	69	74	1	1	-.20	-.16	-.14	2	0	0:00	0:00
11:50	62	67	75	0	1	-.18	-.16	-.14	1	0	0:00	0:00
12:00	67	73	78	1	1	-.24	-.18	-.14	2	0	0:00	0:00
12:10	66	69	72	0	0	-.18	-.16	-.14	0	0	0:00	0:00
12:20	63	68	74	1	3	-.18	-.18	-.14	2	0	0:00	0:00
12:30	67	72	76	1	0	-.20	-.18	-.16	1	0	0:00	0:00
12:40	68	73	77	1	2	-.18	-.18	-.14	0	0	0:00	0:00
12:50	66	70	75	1	0	-.18	-.16	-.12	0	0	0:00	0:00
1:00	67	72	75	0	0	-.18	-.16	-.12	0	0	0:00	0:00
1:10	69	73	77	1	0	-.16	-.16	-.14	1	0	0:00	0:00
1:20	70	73	77	0	0	-.16	-.16	-.14	0	0	0:00	0:00
1:30	68	73	79	1	3	-.16	-.16	-.14	2	0	0:00	0:00
1:40	71	76	82	0	1	-.22	-.18	-.14	0	0	0:00	0:00
1:50	70	75	82	1	0	-.24	-.20	-.16	0	0	0:00	0:00
2:00	67	74	81	2	3	-.24	-.20	-.16	1	0	0:00	0:00
2:10	66	72	76	1	1	-.20	-.18	-.14	0	0	0:00	0:00
2:20	70	79	85	1	0	-.24	-.20	-.14	0	0	0:00	0:00
2:30	68	75	83	0	1	-.22	-.18	-.14	0	0	0:00	0:00
2:40	68	72	77	0	0	-.18	-.16	-.14	0	0	0:00	0:00
2:50	68	72	82	1	2	-.20	-.18	-.12	0	0	0:00	0:00
3:00	64	69	75	1	2	-.20	-.18	-.14	0	0	0:00	0:00
3:10	64	68	72	0	0	-.20	-.20	-.16	0	0	0:00	0:00
3:20	62	68	74	2	1	-.22	-.20	-.18	0	0	0:00	0:00
3:30	63	70	72	0	1	-.20	-.20	-.18	0	0	0:00	0:00
3:40	65	70	73	0	0	-.20	-.20	-.16	0	0	0:00	0:00
3:50	66	71	74	0	2	-.20	-.20	-.18	0	0	0:00	0:00
4:00	66	72	74	0	0	-.20	-.20	-.18	0	0	0:00	0:00
4:10	60	72	83	0	3	-.22	-.20	-.18	0	0	0:00	0:00
4:20	64	75	83	1	0	-.20	-.20	-.18	0	0	0:00	0:00
4:30	63	75	82	0	0	-.22	-.20	-.18	0	0	0:00	0:00
4:40	70	75	78	1	0	-.20	-.20	-.18	0	0	0:00	0:00
4:50	72	76	83	0	1	-.20	-.20	-.18	0	0	0:00	0:00
5:00	71	76	81	0	0	-.20	-.20	-.18	0	0	0:00	0:00
5:10	77	85	93	0	3	-.24	-.20	-.14	0	0	0:00	0:00
5:20	75	80	95	0	0	-.22	-.20	-.18	0	0	0:00	0:00
5:30	76	78	81	0	0	-.20	-.20	-.18	0	0	0:00	0:00
5:40	71	75	81	0	0	-.22	-.20	-.16	0	0	0:00	0:00
5:50	71	75	80	0	0	-.20	-.20	-.18	0	0	0:00	0:00
6:00	72	78	84	2	1	-.22	-.20	-.16	0	0	0:00	0:00
6:10	71	75	78	0	0	-.18	-.18	-.16	0	0	0:00	0:00
6:20	73	76	79	0	0	-.20	-.18	-.16	0	0	0:00	0:00
6:30	75	78	82	1	1	-.18	-.18	-.16	0	0	0:00	0:00

ETC.

FIG.18H

Patient: 5 Feb 81

R-R Interval Distribution Log:

R-R Interval (MS)	All QRS Complexes	Premature Atypical Complexes
up to 224	0	0
225- 248	0	0
249- 272	0	0
273- 296	0	0
297- 328	0	0
329- 352	0	0
353- 376	3	0
377- 400	4	0
401- 424	10	3
425- 448	9	2
449- 472	13	4
473- 496	39	12
497- 529	136	49
529- 552	225	75
553- 576	168	27
577- 600	180	11
601- 624	200	6
625- 648	317	6
649- 672	539	4
673- 696	1818	2
697- 728	4562	5
729- 752	16561	4
753- 776	16630	3
777- 800	18509	3
801- 824	17112	0
825- 848	10035	0
849- 872	6520	0
873- 896	4877	0
897- 928	3133	1
929- 952	1709	0
953- 976	567	2
977-1000	277	0
1001-1024	149	0
1025-1048	114	0
1049-1072	86	0
1073-1096	61	0
1097-1128	54	0

R-R Interval (MS)	All QRS Complexes	Premature Atypical Complexes
1129-1152	46	0
1153-1176	21	0
1177-1200	13	0
1201-1224	8	0
1225-1248	11	0
1249-1272	4	0
1273-1296	7	0
1297-1328	3	0
1329-1352	4	0
1353-1376	1	0
1377-1400	4	0
1401-1424	0	0
1425-1448	5	0
1449-1472	1	0
1473-1496	1	0
1497-1528	0	0
1529-1552	0	0
1553-1576	1	0
1577-1600	0	0
1601-1624	0	0
1625-1648	0	0
1649-1672	0	0
1673-1696	0	0
1697-1728	0	0
1729-1752	0	0
1753-1776	0	0
1777-1800	0	0
1801-1824	0	0
1825-1288	0	0
1289-1872	0	0
1873-1896	0	0
1897-1929	0	0
1929-1952	0	0
1953-1976	0	0
1977-2000	0	0
2000 plus	0	0

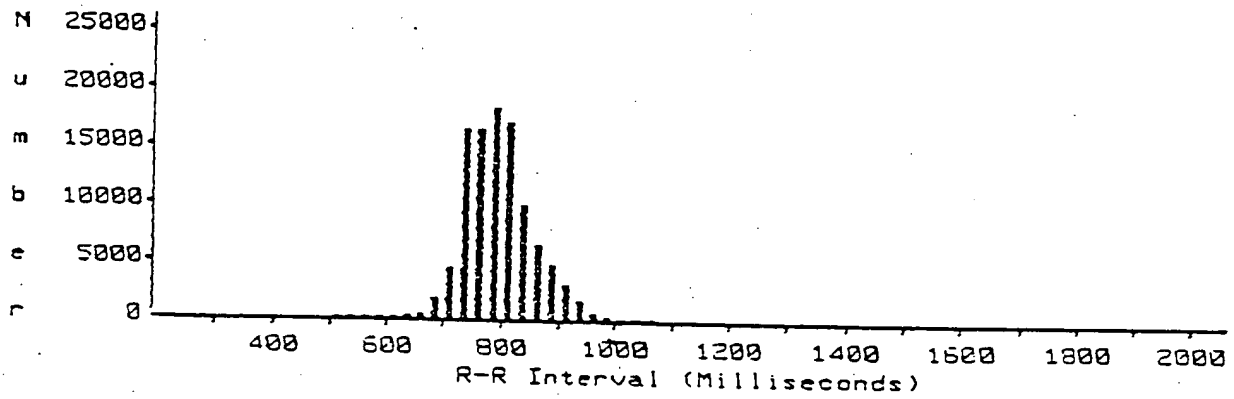
FIG.18I

Patient:

5 Feb 81

R-R Interval Distribution

All QRS Complexes



R-R Interval Distribution

Premature Atypical Complexes

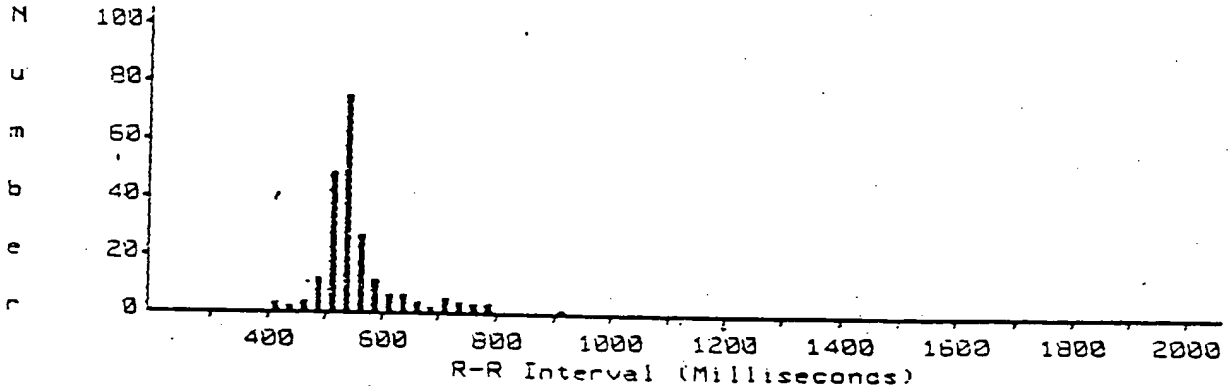


FIG.18J

INTERNATIONAL SEARCH REPORT

International Application No PCT/US81/00419

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC CL.[3] A61B 5/04
US CL. 128 710

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	128/689,690,695,696,202,703,704,705,706,710,711, 419P6, 419P5

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

none

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US,A, 3,829,766, Published 13 August,1974 Herz	
A	US,A, 3,909,792, Published 30 September 1975, Harris	
A	US,A, 4,023,564, Published 17 May,1977 Valiquette et al	
X	US,A, 4,083,366, Published 11 April 1978 Gombrich et al	5-6,9-10
A	US,A, 4,125,111, Published 14 November 1978 Hudspeth et al	
A,P	US,A, 4,197,850, Published 15 April 1980 Schulman et al	
A,P	US,A, 4,232,682, Published 11 November 1980, Veth	
X,P	US,A, 4,237,897, Published 09 December 1980, Beane et al	7

* Special categories of cited documents: [15]

"A" document defining the general state of the art
"E" earlier document but published on or after the international filing date
"L" document cited for special reason other than those referred to in the other categories
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but on or after the priority date claimed
"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention
"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 June 1981	10 JUL 1981
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	W.E. Kamm